

GigaDevice Semiconductor Inc.

GD32E230xx
ARM[®] Cortex[®]-M23 32-bit MCU

Datasheet

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1 General description

The GD32E230xx device belongs to the value line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M23 core. The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor delivers high energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier and a 17-cycle divider.

The GD32E230xx device incorporates the ARM® Cortex®-M23 32-bit processor core operating at up to 72 MHz frequency with Flash accesses 0~2 wait states to obtain maximum efficiency. It provides up to 64 KB embedded Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC and one comparator, up to five general 16-bit timers, a basic timer, a PWM advanced timer, as well as standard and advanced communication interfaces: up to two SPIs, two I2Cs, two USARTs, and an I2S.

The device operates from a 1.8 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32E230xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.



2 Device overview

2.1 Device information

Table 2-1. GD32E230xx devices features and peripheral list

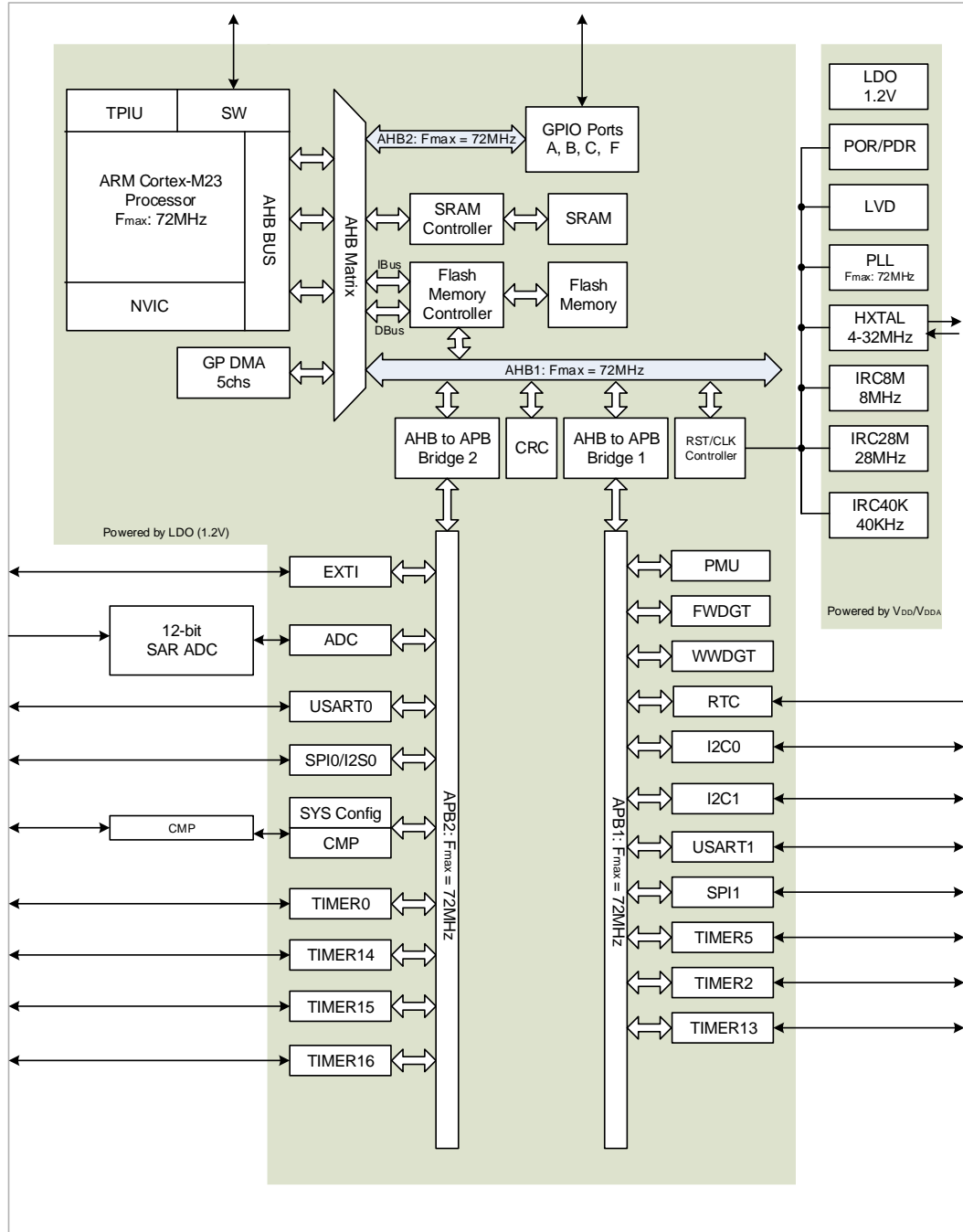
| Part Number | GD32E230xx | | | | | | | | | |
|---------------------|---|----------------------------------|----------------------------------|---------------------------------|----------------------------------|----------------------------------|---------------------------------|----------------------------------|----------------------------------|---------------------------------|
| | K4U6 | K6U6 | K8U6 | K4T6 | K6T6 | K8T6 | C4T6 | C6T6 | C8T6 | |
| FLASH (KB) | 16 | 32 | 64 | 16 | 32 | 64 | 16 | 32 | 64 | |
| SRAM (KB) | 4 | 6 | 8 | 4 | 4 | 8 | 4 | 6 | 8 | |
| Timers | General timer(16-bit) <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 5 <small>(2,13-16)</small> | 4 <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 5 <small>(2,13-16)</small> | 4 <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 5 <small>(2,13-16)</small> |
| | Advanced timer(16-bit) <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Basic timer(16-bit) <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> |
| | I2C <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> |
| | SPI/I2S <small>(0)/(0)</small> | 1/1 <small>(0)/(0)</small> | 1/1 <small>(0)/(0)</small> | 2/1 <small>(0-1)/(0)</small> | 1/1 <small>(0)/(0)</small> | 1/1 <small>(0)/(0)</small> | 2/1 <small>(0-1)/(0)</small> | 1/1 <small>(0)/(0)</small> | 1/1 <small>(0)/(0)</small> | 2/1 <small>(0-1)/(0)</small> |
| GPIO | 27 | 27 | 27 | 25 | 25 | 25 | 39 | 39 | 39 | |
| CMP | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| EXTI | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | |
| ADC | Units | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Channels (External) | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 |
| | Channels (Internal) | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Package | QFN32 | | | LQFP32 | | | LQFP48 | | | |

Table 2-2. GD32E230xx devices features and peripheral list (continued)

| Part Number | GD32E230xx | | | | | | | | | |
|---------------------|---|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|---------------------------------|
| | F4V6 | F6V6 | F8V6 | F4P6 | F6P6 | F8P6 | G4U6 | G6U6 | G8U6 | |
| FLASH (KB) | 16 | 32 | 64 | 16 | 32 | 64 | 16 | 32 | 64 | |
| SRAM (KB) | 4 | 6 | 8 | 4 | 6 | 8 | 4 | 6 | 8 | |
| Timers | General timer(16-bit) <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 4 <small>(2,13,15,16)</small> | 5 <small>(2,13,16)</small> |
| | Advanced timer(16-bit) <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Basic timer(16-bit) <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> | 1 <small>(5)</small> |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> |
| | I2C <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> |
| | SPI/I2S <small>(0)/(0)</small> | 1/1 <small>(0)/(0)</small> | 1/1 <small>(0)/(0)</small> | 2/1 <small>(0-1)/(0)</small> | 1/1 <small>(0)/(0)</small> | 1/1 <small>(0)/(0)</small> | 2/1 <small>(0-1)/(0)</small> | 1/1 <small>(0)/(0)</small> | 1/1 <small>(0)/(0)</small> | 2/1 <small>(0-1)/(0)</small> |
| GPIO | 15 | 15 | 15 | 15 | 15 | 15 | 23 | 23 | 23 | |
| CMP | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| EXTI | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | |
| ADC | Units | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Channels (External) | 9 | 9 | 9 | 9 | 9 | 9 | 10 | 10 | 10 |
| | Channels (Internal) | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Package | LGA20 | | | TSSOP20 | | | QFN28 | | | |

2.2 Block diagram

Figure 2-1. GD32E230xx block diagram



2.3 Pinouts and pin assignment

Figure 2-2. GD32E230Cx LQFP48 pinouts

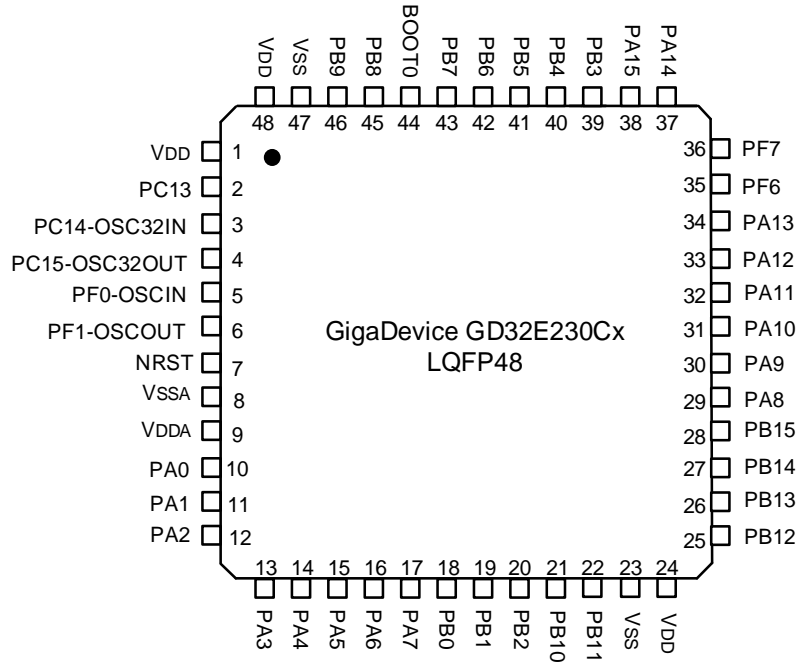


Figure 2-3. GD32E230Kx LQFP32 pinouts

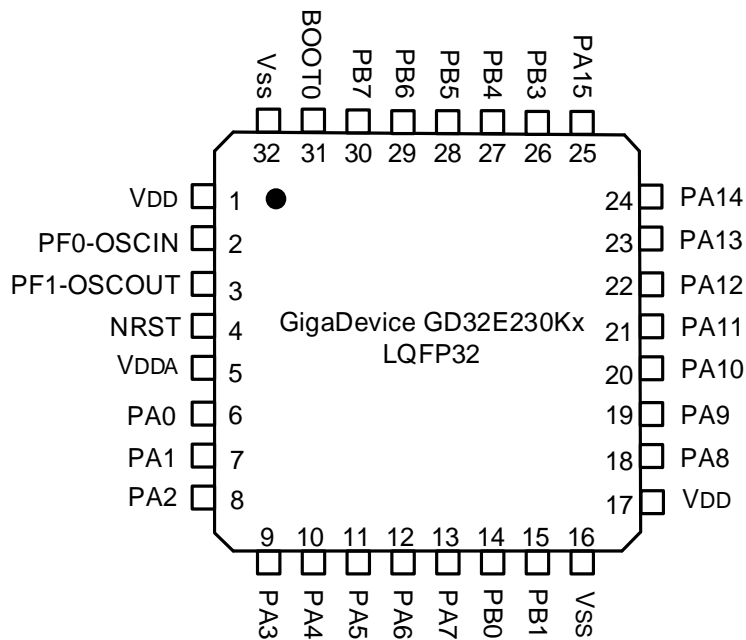


Figure 2-4. GD32E230Kx QFN32 pinouts

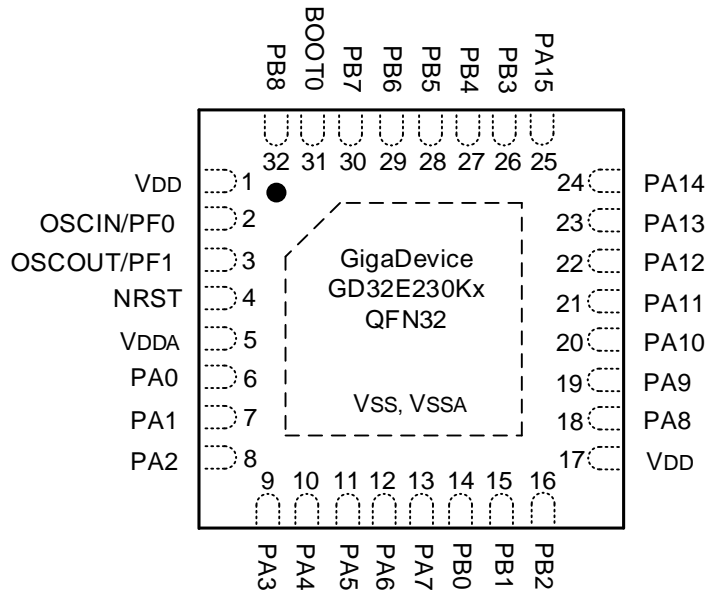


Figure 2-5. GD32E230Gx QFN28 pinouts

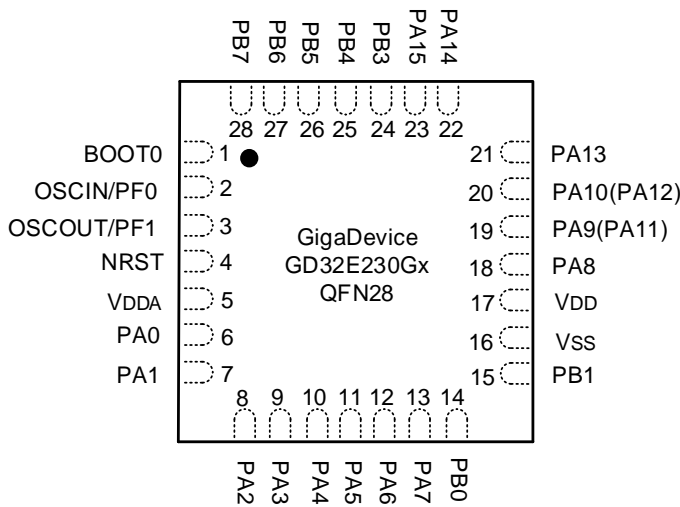


Figure 2-6. GD32E230Fx TSSOP20 pinouts

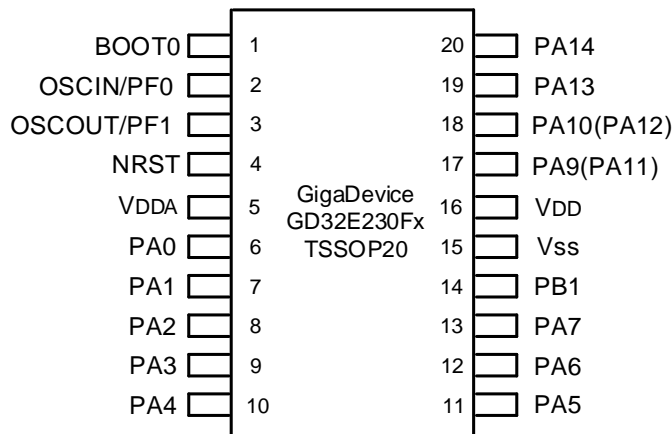
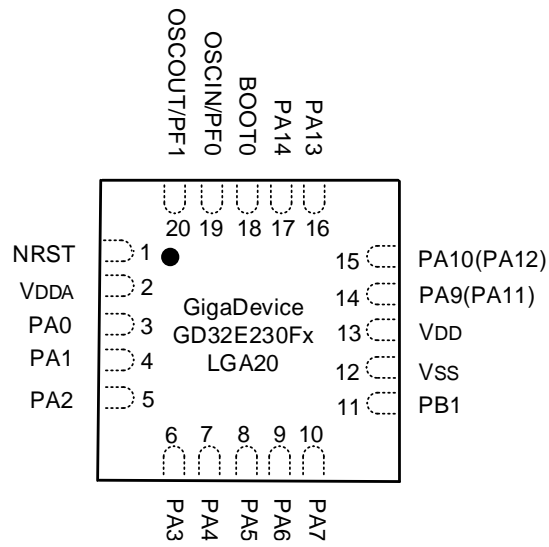


Figure 2-7. GD32E230Fx LGA20 pinouts



2.4 Memory map

Table 2-3. GD32E230xx memory map

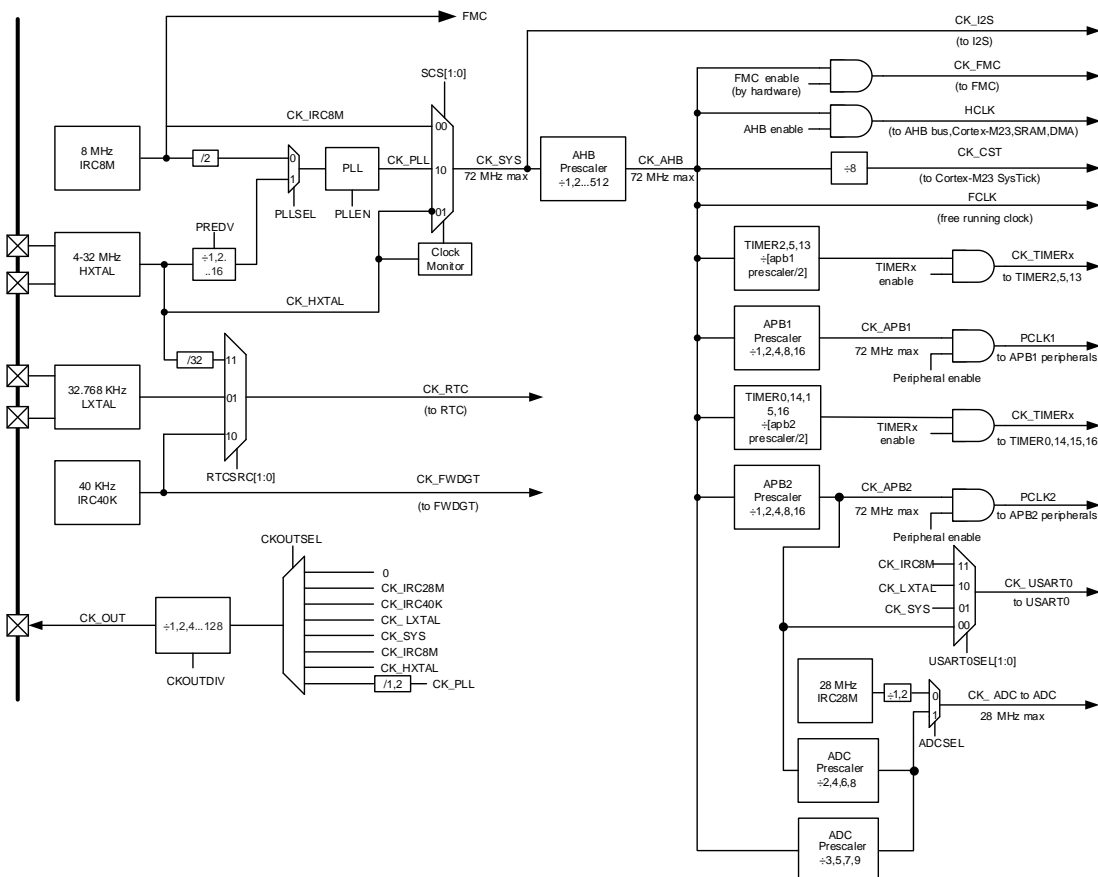
| Pre-defined Regions | Bus | ADDRESS | Peripherals |
|---------------------------|---------------------------|---------------------------|---------------------------------|
| | | 0xE000 0000 - 0xE00F FFFF | Cortex M23 internal peripherals |
| External Device | | 0xA000 0000 - 0xDFFF FFFF | Reserved |
| External RAM | | 0x60000000 - 0x9FFFFFFF | Reserved |
| Peripherals | AHB1 | 0x5004 0000 - 0x5FFF FFFF | Reserved |
| | | 0x5000 0000 - 0x5003 FFFF | Reserved |
| | AHB2 | 0x4800 1800 - 0x4FFF FFFF | Reserved |
| | | 0x4800 1400 - 0x4800 17FF | GPIOF |
| | | 0x4800 1000 - 0x4800 13FF | Reserved |
| | | 0x4800 0C00 - 0x4800 0FFF | Reserved |
| | | 0x4800 0800 - 0x4800 0BFF | GPIOC |
| | | 0x4800 0400 - 0x4800 07FF | GPIOB |
| | | 0x4800 0000 - 0x4800 03FF | GPIOA |
| | AHB1 | 0x4002 4400 - 0x47FF FFFF | Reserved |
| | | 0x4002 4000 - 0x4002 43FF | Reserved |
| | | 0x4002 3400 - 0x4002 3FFF | Reserved |
| | | 0x4002 3000 - 0x4002 33FF | CRC |
| | | 0x4002 2400 - 0x4002 2FFF | Reserved |
| | | 0x4002 2000 - 0x4002 23FF | FMC |
| | | 0x4002 1400 - 0x4002 1FFF | Reserved |
| | | 0x4002 1000 - 0x4002 13FF | RCU |
| | | 0x4002 0400 - 0x4002 0FFF | Reserved |
| | | 0x4002 0000 - 0x4002 03FF | DMA |
| | APB2 | 0x4001 8000 - 0x4001 FFFF | Reserved |
| | | 0x4001 5C00 - 0x4001 7FFF | Reserved |
| | | 0x4001 5800 - 0x4001 5BFF | DBG |
| | | 0x4001 4C00 - 0x4001 57FF | Reserved |
| | | 0x4001 4800 - 0x4001 4BFF | TIMER16 |
| | | 0x4001 4400 - 0x4001 47FF | TIMER15 |
| | | 0x4001 4000 - 0x4001 43FF | TIMER14 |
| | | 0x4001 3C00 - 0x4001 3FFF | Reserved |
| | | 0x4001 3800 - 0x4001 3BFF | USART0 |
| | | 0x4001 3400 - 0x4001 37FF | Reserved |
| | | 0x4001 3000 - 0x4001 33FF | SPI0/I2S0 |
| | | 0x4001 2C00 - 0x4001 2FFF | TIMER0 |
| | | 0x4001 2800 - 0x4001 2BFF | Reserved |
| | 0x4001 2400 - 0x4001 27FF | ADC | |
| 0x4001 0800 - 0x4001 23FF | Reserved | | |

| Pre-defined Regions | Bus | ADDRESS | Peripherals |
|---------------------|------|---------------------------|-------------------|
| | | 0x4001 0400 - 0x4001 07FF | EXTI |
| | | 0x4001 0000 - 0x4001 03FF | SYSCFG + CMP |
| | APB1 | 0x4000 CC00 - 0x4000 FFFF | Reserved |
| | | 0x4000 C800 - 0x4000 CBFF | Reserved |
| | | 0x4000 C400 - 0x4000 C7FF | Reserved |
| | | 0x4000 C000 - 0x4000 C3FF | Reserved |
| | | 0x4000 8000 - 0x4000 BFFF | Reserved |
| | | 0x4000 7C00 - 0x4000 7FFF | Reserved |
| | | 0x4000 7800 - 0x4000 7BFF | Reserved |
| | | 0x4000 7400 - 0x4000 77FF | Reserved |
| | | 0x4000 7000 - 0x4000 73FF | PMU |
| | | 0x4000 6400 - 0x4000 6FFF | Reserved |
| | | 0x4000 6000 - 0x4000 63FF | Reserved |
| | | 0x4000 5C00 - 0x4000 5FFF | Reserved |
| | | 0x4000 5800 - 0x4000 5BFF | I2C1 |
| | | 0x4000 5400 - 0x4000 57FF | I2C0 |
| | | 0x4000 4800 - 0x4000 53FF | Reserved |
| | | 0x4000 4400 - 0x4000 47FF | USART1 |
| | | 0x4000 4000 - 0x4000 43FF | Reserved |
| | | 0x4000 3C00 - 0x4000 3FFF | Reserved |
| | | 0x4000 3800 - 0x4000 3BFF | SPI1 |
| | | 0x4000 3400 - 0x4000 37FF | Reserved |
| | | 0x4000 3000 - 0x4000 33FF | FWDGT |
| | | 0x4000 2C00 - 0x4000 2FFF | WWDGT |
| | | 0x4000 2800 - 0x4000 2BFF | RTC |
| | | 0x4000 2400 - 0x4000 27FF | Reserved |
| | | 0x4000 2000 - 0x4000 23FF | TIMER13 |
| | | 0x4000 1400 - 0x4000 1FFF | Reserved |
| | | 0x4000 1000 - 0x4000 13FF | TIMER5 |
| | | 0x4000 0800 - 0x4000 0FFF | Reserved |
| | | 0x4000 0400 - 0x4000 07FF | TIMER2 |
| | | 0x4000 0000 - 0x4000 03FF | Reserved |
| SRAM | | 0x2000 2000 - 0x3FFF FFFF | Reserved |
| | | 0x2000 0000 - 0x2000 1FFF | SRAM |
| Code | | 0x1FFF F810 - 0x1FFF FFFF | Reserved |
| | | 0x1FFF F800 - 0x1FFF F80F | Option bytes |
| | | 0x1FFF EC00 - 0x1FFF F7FF | System memory |
| | | 0x0801 0000 - 0x1FFF EBFF | Reserved |
| | | 0x0800 0000 - 0x0800 FFFF | Main Flash memory |
| | | 0x0001 0000 - 0x07FF FFFF | Reserved |

| Pre-defined Regions | Bus | ADDRESS | Peripherals |
|---------------------|-----|-------------------------|-----------------------------------|
| | | 0x00000000 - 0x0000FFFF | Aliased to Flash or system memory |

2.5 Clock tree

Figure 2-8. GD32E230xx clock tree



Note:

If the APB prescaler is 1, the timer clock frequencies are set to AHB frequency divide by 1. Otherwise, they are set to the AHB frequency divide by half of APB prescaler.

Legend:

- HXTAL: High speed crystal oscillator
- LXTAL: Low speed crystal oscillator
- IRC8M: Internal 8M RC oscillator
- IRC40K: Internal 40K RC oscillator
- IRC28M: Internal 28M RC oscillator

2.6 Pin definitions

2.6.1 GD32E230Cx LQFP48 pin definitions

Table 2-4. GD32E230Cx LQFP48 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|------------------|------|-------------------------|--------------------------|---|
| V _{DD} | 1 | P | | Default: V _{DD} |
| PC13-TAMPER-RTC | 2 | I/O | | Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1 |
| PC14-OSC32IN | 3 | I/O | | Default: PC14 Additional: OSC32IN |
| PC15-OSC32OUT | 4 | I/O | | Default: PC15 Additional: OSC32OUT |
| PF0-OSCIN | 5 | I/O | 5VT | Default: PF0 Alternate: I2C0_SDA Additional: OSCIN |
| PF1-OSCOU | 6 | I/O | 5VT | Default: PF1 Alternate: I2C0_SCL Additional: OSCOUT |
| NRST | 7 | I/O | | Default: NRST |
| V _{SSA} | 8 | P | | Default: V _{SSA} |
| V _{DDA} | 9 | P | | Default: V _{DDA} |
| PA0-WKUP | 10 | I/O | | Default: PA0 Alternate: USART0_CTS ⁽³⁾ , USART1_CTS ⁽⁴⁾ , CMP_OUT, I2C1_SCL ⁽⁵⁾ Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0 |
| PA1 | 11 | I/O | | Default: PA1 Alternate: USART0_RTS ⁽³⁾ , USART1_RTS ⁽⁴⁾ , I2C1_SDA ⁽⁵⁾ , EVENTOUT, TIMER14_CH0_ON ⁽⁵⁾ Additional: ADC_IN1, CMP_IP |
| PA2 | 12 | I/O | | Default: PA2 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , TIMER14_CH0 ⁽⁵⁾ Additional: ADC_IN2, CMP_IM7 |
| PA3 | 13 | I/O | | Default: PA3 Alternate: USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER14_CH1 ⁽⁵⁾ Additional: ADC_IN3 |
| PA4 | 14 | I/O | | Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK ⁽³⁾ , USART1_CK ⁽⁴⁾ , TIMER13_CH0, SPI1_NSS ⁽⁵⁾ Additional: ADC_IN4, CMP_IM4 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-----------------|------|-------------------------|--------------------------|---|
| PA5 | 15 | I/O | | Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5, CMP_IM5 |
| PA6 | 16 | I/O | | Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT Additional: ADC_IN6 |
| PA7 | 17 | I/O | | Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7 |
| PB0 | 18 | I/O | | Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX ⁽⁴⁾ , EVENTOUT Additional: ADC_IN8 |
| PB1 | 19 | I/O | | Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK ⁽⁵⁾ Additional: ADC_IN9 |
| PB2 | 20 | I/O | 5VT | Default: PB2 Alternate: TIMER2_ETI |
| PB10 | 21 | I/O | 5VT | Default: PB10 Alternate: I2C0_SCL ⁽³⁾ , I2C1_SCL ⁽⁵⁾ , SPI1_IO2 ⁽⁵⁾ , SPI1_SCK ⁽⁵⁾ |
| PB11 | 22 | I/O | 5VT | Default: PB11 Alternate: I2C0_SDA ⁽³⁾ , I2C1_SDA ⁽⁵⁾ , EVENTOUT, SPI1_IO3 ⁽⁵⁾ |
| V _{SS} | 23 | P | | Default: V _{SS} |
| V _{DD} | 24 | P | | Default: V _{DD} |
| PB12 | 25 | I/O | 5VT | Default: PB12 Alternate: SPI0_NSS ⁽³⁾ , SPI1_NSS ⁽⁵⁾ , TIMER0_BRKIN, I2C1_SMBA ⁽⁵⁾ , EVENTOUT |
| PB13 | 26 | I/O | 5VT | Default: PB13 Alternate: SPI0_SCK ⁽³⁾ , SPI1_SCK ⁽⁵⁾ , TIMER0_CH0_ON, I2C1_TXFRAME ⁽⁵⁾ , I2C1_SCL ⁽⁵⁾ |
| PB14 | 27 | I/O | 5VT | Default: PB14 Alternate: SPI0_MISO ⁽³⁾ , SPI1_MISO ⁽⁵⁾ , TIMER0_CH1_ON, TIMER14_CH0 ⁽⁵⁾ , I2C1_SDA ⁽⁵⁾ |
| PB15 | 28 | I/O | 5VT | Default: PB15 Alternate: SPI0_MOSI ⁽³⁾ , SPI1_MOSI ⁽⁵⁾ , TIMER0_CH2_ON, TIMER14_CH0_ON ⁽⁵⁾ , TIMER14_CH1 ⁽⁵⁾ Additional: RTC_REFIN, WKUP6 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|---|
| PA8 | 29 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX ⁽⁴⁾ , EVENTOUT |
| PA9 | 30 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN ⁽⁵⁾ , I2C0_SCL, CK_OUT |
| PA10 | 31 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA |
| PA11 | 32 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, CMP_OUT, EVENTOUT, SPI1_IO2 ⁽⁵⁾ , I2C0_SMBA, I2C1_SCL ⁽⁵⁾ |
| PA12 | 33 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT, SPI1_IO3 ⁽⁵⁾ , I2C0_TXFRAME, I2C1_SDA ⁽⁵⁾ |
| PA13 | 34 | I/O | 5VT | Default: PA13 Alternate: SWDIO, IFRP_OUT, SPI1_MISO ⁽⁵⁾ |
| PF6 | 35 | I/O | 5VT | Default: PF6 Alternate: I2C0_SCL ⁽³⁾ , I2C1_SCL ⁽⁵⁾ |
| PF7 | 36 | I/O | 5VT | Default: PF7 Alternate: I2C0_SDA ⁽³⁾ , I2C1_SDA ⁽⁵⁾ |
| PA14 | 37 | I/O | 5VT | Default: PA14 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , SWCLK, SPI1_MOSI ⁽⁵⁾ |
| PA15 | 38 | I/O | 5VT | Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , SPI1_NSS ⁽⁵⁾ , EVENTOUT |
| PB3 | 39 | I/O | 5VT | Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT |
| PB4 | 40 | I/O | 5VT | Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT, I2C0_TXFRAME, TIMER16_BRKIN |
| PB5 | 41 | I/O | 5VT | Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 Additional: WKUP5 |
| PB6 | 42 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON |
| PB7 | 43 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON |
| BOOT0 | 44 | I | | Default: BOOT0 |
| PB8 | 45 | I/O | 5VT | Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0 |
| PB9 | 46 | I/O | 5VT | Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-----------------|------|-------------------------|--------------------------|---|
| | | | | EVENTOUT, I2S0_MCK, SPI1_NSS ⁽⁵⁾ |
| V _{SS} | 47 | P | | Default: V _{SS} |
| V _{DD} | 48 | P | | Default: V _{DD} |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32E230C4 devices only.
- (4) Functions are available on GD32E230C8/6 devices.
- (5) Functions are available on GD32E230C8 devices only.

2.6.2 GD32E230Kx LQFP32 pin definitions

Table 2-5. GD32E230Kx LQFP32 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|------------------|------|-------------------------|--------------------------|---|
| V _{DD} | 1 | P | | Default: V _{DD} |
| PF0-OSCIN | 2 | I/O | 5VT | Default: PF0 Alternate: I2C0_SDA Additional: OSCIN |
| PF1-OSCOU | 3 | I/O | 5VT | Default: PF1 Alternate: I2C0_SCL Additional: OSCOUT |
| NRST | 4 | I/O | | Default: NRST |
| V _{DDA} | 5 | P | | Default: V _{DDA} |
| PA0-WKUP | 6 | I/O | | Default: PA0 Alternate: USART0_CTS ⁽³⁾ , USART1_CTS ⁽⁴⁾ , CMP_OUT, I2C1_SCL ⁽⁵⁾ Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0 |
| PA1 | 7 | I/O | | Default: PA1 Alternate: USART0_RTS ⁽³⁾ , USART1_RTS ⁽⁴⁾ , I2C1_SDA ⁽⁵⁾ , EVENTOUT, TIMER14_CH0_ON ⁽⁵⁾ Additional: ADC_IN1, CMP_IP |
| PA2 | 8 | I/O | | Default: PA2 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , TIMER14_CH0 ⁽⁵⁾ Additional: ADC_IN2, CMP_IM7 |
| PA3 | 9 | I/O | | Default: PA3 Alternate: USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER14_CH1 ⁽⁵⁾ Additional: ADC_IN3 |
| PA4 | 10 | I/O | | Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK ⁽³⁾ , USART1_CK ⁽⁴⁾ , TIMER13_CH0, SPI1_NSS ⁽⁵⁾ |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-----------------|------|-------------------------|--------------------------|---|
| | | | | Additional: ADC_IN4, CMP_IM4 |
| PA5 | 11 | I/O | | Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5, CMP_IM5 |
| PA6 | 12 | I/O | | Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT Additional: ADC_IN6 |
| PA7 | 13 | I/O | | Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7 |
| PB0 | 14 | I/O | | Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX ⁽⁴⁾ , EVENTOUT Additional: ADC_IN8 |
| PB1 | 15 | I/O | | Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK ⁽⁵⁾ Additional: ADC_IN9 |
| V _{SS} | 16 | P | | Default: V _{SS} |
| V _{DD} | 17 | P | | Default: V _{DD} |
| PA8 | 18 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX ⁽⁴⁾ , EVENTOUT |
| PA9 | 19 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN ⁽⁵⁾ , I2C0_SCL, CK_OUT |
| PA10 | 20 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA |
| PA11 | 21 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, CMP_OUT, EVENTOUT, SPI1_IO2 ⁽⁵⁾ , I2C0_SMBA, I2C1_SCL ⁽⁵⁾ |
| PA12 | 22 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT, SPI1_IO3 ⁽⁵⁾ , I2C0_TXFRAME, I2C1_SDA ⁽⁵⁾ |
| PA13 | 23 | I/O | 5VT | Default: PA13 Alternate: SWDIO, IFRP_OUT, SPI1_MISO ⁽⁵⁾ |
| PA14 | 24 | I/O | 5VT | Default: PA14 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , SWCLK, SPI1_MOSI ⁽⁵⁾ |
| PA15 | 25 | I/O | 5VT | Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-----------------|------|-------------------------|--------------------------|--|
| | | | | USART1_RX ⁽⁴⁾ , SPI1_NSS ⁽⁵⁾ , EVENTOUT |
| PB3 | 26 | I/O | 5VT | Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT |
| PB4 | 27 | I/O | 5VT | Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT, I2C0_TXFRAME, TIMER16_BRKIN |
| PB5 | 28 | I/O | 5VT | Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 Additional: WKUP5 |
| PB6 | 29 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON |
| PB7 | 30 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON |
| BOOT0 | 31 | I | | Default: BOOT0 |
| V _{SS} | 32 | P | | Default: V _{SS} |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32E230K4 devices only.
- (4) Functions are available on GD32E230K8/6 devices.
- (5) Functions are available on GD32E230K8 devices only.

2.6.3 GD32E230Kx QFN32 pin definitions

Table 2-6. GD32E230Kx QFN32 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|------------------|------|-------------------------|--------------------------|---|
| V _{DD} | 1 | P | | Default: V _{DD} |
| PF0-OSCIN | 2 | I/O | 5VT | Default: PF0 Alternate: I2C0_SDA Additional: OSCIN |
| PF1-OSCOU | 3 | I/O | 5VT | Default: PF1 Alternate: I2C0_SCL Additional: OSCOUT |
| NRST | 4 | I/O | | Default: NRST |
| V _{DDA} | 5 | P | | Default: V _{DDA} |
| PA0-WKUP | 6 | I/O | | Default: PA0 Alternate: USART0_CTS ⁽³⁾ , USART1_CTS ⁽⁴⁾ , CMP_OUT, I2C1_SCL ⁽⁵⁾ Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0 |
| PA1 | 7 | I/O | | Default: PA1 Alternate: USART0_RTS ⁽³⁾ , USART1_RTS ⁽⁴⁾ , I2C1_SDA ⁽⁵⁾ , EVENTOUT, TIMER14_CH0_ON ⁽⁵⁾ |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-----------------|------|-------------------------|--------------------------|---|
| | | | | Additional: ADC_IN1, CMP_IP |
| PA2 | 8 | I/O | | Default: PA2 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , TIMER14_CH0 ⁽⁵⁾ Additional: ADC_IN2, CMP_IM7 |
| PA3 | 9 | I/O | | Default: PA3 Alternate: USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER14_CH1 ⁽⁵⁾ Additional: ADC_IN3 |
| PA4 | 10 | I/O | | Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK ⁽³⁾ , USART1_CK ⁽⁴⁾ , TIMER13_CH0, SPI1_NSS ⁽⁵⁾ Additional: ADC_IN4, CMP_IM4 |
| PA5 | 11 | I/O | | Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5, CMP_IM5 |
| PA6 | 12 | I/O | | Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT Additional: ADC_IN6 |
| PA7 | 13 | I/O | | Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7 |
| PB0 | 14 | I/O | | Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX ⁽⁴⁾ , EVENTOUT Additional: ADC_IN8 |
| PB1 | 15 | I/O | | Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK ⁽⁵⁾ Additional: ADC_IN9 |
| PB2 | 16 | I/O | 5VT | Default: PB2 Alternate: TIMER2_ETI |
| V _{DD} | 17 | P | | Default: V _{DD} |
| PA8 | 18 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX ⁽⁴⁾ , EVENTOUT |
| PA9 | 19 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN ⁽⁵⁾ , I2C0_SCL, CK_OUT |
| PA10 | 20 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|---|
| PA11 | 21 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, CMP_OUT, EVENTOUT, SPI1_IO2 ⁽⁵⁾ , I2C0_SMBA, I2C1_SCL ⁽⁵⁾ |
| PA12 | 22 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT, SPI1_IO3 ⁽⁵⁾ , I2C0_TXFRAME, I2C1_SDA ⁽⁵⁾ |
| PA13 | 23 | I/O | 5VT | Default: PA13 Alternate: SWDIO, IFRP_OUT, SPI1_MISO ⁽⁵⁾ |
| PA14 | 24 | I/O | 5VT | Default: PA14 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , SWCLK, SPI1_MOSI ⁽⁵⁾ |
| PA15 | 25 | I/O | 5VT | Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , SPI1_NSS ⁽⁵⁾ , EVENTOUT |
| PB3 | 26 | I/O | 5VT | Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT |
| PB4 | 27 | I/O | 5VT | Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT, I2C0_TXFRAME, TIMER16_BRKIN |
| PB5 | 28 | I/O | 5VT | Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 Additional: WKUP5 |
| PB6 | 29 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON |
| PB7 | 30 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON |
| BOOT0 | 31 | I | | Default: BOOT0 |
| PB8 | 32 | I/O | 5VT | Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0 |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32E230K4 devices only.
- (4) Functions are available on GD32E230K8/6 devices.
- (5) Functions are available on GD32E230K8 devices only.

2.6.4 GD32E230Gx QFN28 pin definitions

Table 2-7. GD32E230Gx QFN28 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-----------|------|-------------------------|--------------------------|-----------------------|
| BOOT0 | 1 | I | | Default: BOOT0 |
| PF0-OSCIN | 2 | I/O | 5VT | Default: PF0 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|------------------|------|-------------------------|--------------------------|--|
| | | | | Alternate: I2C0_SDA Additional: OSCIN |
| PF1- OSCOUT | 3 | I/O | 5VT | Default: PF1 Alternate: I2C0_SCL Additional: OSCOUT |
| NRST | 4 | I/O | | Default: NRST |
| V _{DDA} | 5 | P | | Default: V _{DDA} |
| PA0-WKUP | 6 | I/O | | Default: PA0 Alternate: USART0_CTS ⁽³⁾ , USART1_CTS ⁽⁴⁾ , CMP_OUT, I2C1_SCL ⁽⁵⁾ Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0 |
| PA1 | 7 | I/O | | Default: PA1 Alternate: USART0_RTS ⁽³⁾ , USART1_RTS ⁽⁴⁾ , I2C1_SDA ⁽⁵⁾ , EVENTOUT, TIMER14_CH0_ON ⁽⁵⁾ Additional: ADC_IN1, CMP_IP |
| PA2 | 8 | I/O | | Default: PA2 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , TIMER14_CH0 ⁽⁵⁾ Additional: ADC_IN2, CMP_IM7 |
| PA3 | 9 | I/O | | Default: PA3 Alternate: USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER14_CH1 ⁽⁵⁾ Additional: ADC_IN3 |
| PA4 | 10 | I/O | | Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK ⁽³⁾ , USART1_CK ⁽⁴⁾ , TIMER13_CH0, SPI1_NSS ⁽⁵⁾ Additional: ADC_IN4, CMP_IM4 |
| PA5 | 11 | I/O | | Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5, CMP_IM5 |
| PA6 | 12 | I/O | | Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT Additional: ADC_IN6 |
| PA7 | 13 | I/O | | Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7 |
| PB0 | 14 | I/O | | Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX ⁽⁴⁾ , EVENTOUT Additional: ADC_IN8 |
| PB1 | 15 | I/O | | Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|---------------------|------|-------------------------|--------------------------|---|
| | | | | TIMER0_CH2_ON, SPI1_SCK ⁽⁵⁾ Additional: ADC_IN9 |
| V _{SS} | 16 | P | | Default: V _{SS} |
| V _{DD} | 17 | P | | Default: V _{DD} |
| PA8 | 18 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX ⁽⁴⁾ , EVENTOUT |
| PA9 ⁽⁶⁾ | 19 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN ⁽⁵⁾ , I2C0_SCL, CK_OUT |
| PA10 ⁽⁶⁾ | 20 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA |
| PA13 | 21 | I/O | 5VT | Default: PA13 Alternate: SWDIO, IFRP_OUT, SPI1_MISO ⁽⁵⁾ |
| PA14 | 22 | I/O | 5VT | Default: PA14 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , SWCLK, SPI1_MOSI ⁽⁵⁾ |
| PA15 | 23 | I/O | 5VT | Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , SPI1_NSS ⁽⁵⁾ , EVENTOUT |
| PB3 | 24 | I/O | 5VT | Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT |
| PB4 | 25 | I/O | 5VT | Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT, I2C0_TXFRAME, TIMER16_BRKIN |
| PB5 | 26 | I/O | 5VT | Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 Additional: WKUP5 |
| PB6 | 27 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON |
| PB7 | 28 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32E230G4 devices only.
- (4) Functions are available on GD32E230G8/6 devices.
- (5) Functions are available on GD32E230G8 devices only.
- (6) Pin pair PA11/PA12 can be remapped instead of pin pair PA9/PA10 using SYSCFG_CFG0 register. [Table 2-10. Port A alternate functions summary](#) shows PA11/PA12 remap.

2.6.5 GD32E230Fx TSSOP20 pin definitions
Table 2-8. GD32E230Fx TSSOP20 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|------------------|------|-------------------------|--------------------------|--|
| PF0-OSCIN | 2 | I/O | 5VT | Default: PF0 Alternate: I2C0_SDA Additional: OSCIN |
| PF1-OSCOU | 3 | I/O | 5VT | Default: PF1 Alternate: I2C0_SCL Additional: OSCOUT |
| NRST | 4 | I/O | | Default: NRST |
| V _{DDA} | 5 | P | | Default: V _{DDA} |
| PA0-WKUP | 6 | I/O | | Default: PA0 Alternate: USART0_CTS ⁽³⁾ , USART1_CTS ⁽⁴⁾ , CMP_OUT, I2C1_SCL ⁽⁵⁾ Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0 |
| PA1 | 7 | I/O | | Default: PA1 Alternate: USART0_RTS ⁽³⁾ , USART1_RTS ⁽⁴⁾ , I2C1_SDA ⁽⁵⁾ , EVENTOUT Additional: ADC_IN1, CMP_IP |
| PA2 | 8 | I/O | | Default: PA2 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ Additional: ADC_IN2, CMP_IM7 |
| PA3 | 9 | I/O | | Default: PA3 Alternate: USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ Additional: ADC_IN3 |
| PA4 | 10 | I/O | | Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK ⁽³⁾ , USART1_CK ⁽⁴⁾ , TIMER13_CH0, SPI1_NSS ⁽⁵⁾ Additional: ADC_IN4, CMP_IM4 |
| PA5 | 11 | I/O | | Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5, CMP_IM5 |
| PA6 | 12 | I/O | | Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT Additional: ADC_IN6 |
| PA7 | 13 | I/O | | Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7 |
| PB1 | 14 | I/O | | Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK ⁽⁵⁾ |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|---------------------|------|-------------------------|--------------------------|---|
| | | | | Additional: ADC_IN9 |
| V _{SS} | 15 | P | | Default: V _{SS} |
| V _{DD} | 16 | P | | Default: V _{DD} |
| PA9 ⁽⁶⁾ | 17 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, I2C0_SCL, CK_OUT |
| PA10 ⁽⁶⁾ | 18 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA |
| PA13 | 19 | I/O | 5VT | Default: PA13 Alternate: SWDIO, IFRP_OUT, SPI1_MISO ⁽⁵⁾ |
| PA14 | 20 | I/O | 5VT | Default: PA14 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , SWCLK, SPI1_MOSI ⁽⁵⁾ |
| BOOT0 | 1 | I | | Default: BOOT0 |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32E230F4 devices only.
- (4) Functions are available on GD32E230F8/6 devices.
- (5) Functions are available on GD32E230F8 devices only.
- (6) Pin pair PA11/PA12 can be remapped instead of pin pair PA9/PA10 using SYSCFG_CFG0 register. [Table 2-10. Port A alternate functions summary](#) shows PA11/PA12 remap.

2.6.6 GD32E230Fx LGA20 pin definitions

Table 2-9. GD32E230Fx LGA20 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|------------------|------|-------------------------|--------------------------|---|
| PF0-OSCIN | 19 | I/O | 5VT | Default: PF0 Alternate: I2C0_SDA Additional: OSCIN |
| PF1-OSCOU | 20 | I/O | 5VT | Default: PF1 Alternate: I2C0_SCL Additional: OSCOUT |
| NRST | 1 | I/O | | Default: NRST |
| V _{DDA} | 2 | P | | Default: V _{DDA} |
| PA0-WKUP | 3 | I/O | | Default: PA0 Alternate: USART0_CTS ⁽³⁾ , USART1_CTS ⁽⁴⁾ , CMP_OUT, I2C1_SCL ⁽⁵⁾ Additional: ADC_IN0, CMP_IM6, RTC_TAMP1, WKUP0 |
| PA1 | 4 | I/O | | Default: PA1 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|---------------------|------|-------------------------|--------------------------|--|
| | | | | Alternate: USART0_RTS ⁽³⁾ , USART1_RTS ⁽⁴⁾ , I2C1_SDA ⁽⁵⁾ , EVENTOUT Additional: ADC_IN1, CMP_IP |
| PA2 | 5 | I/O | | Default: PA2 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ Additional: ADC_IN2, CMP_IM7 |
| PA3 | 6 | I/O | | Default: PA3 Alternate: USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ Additional: ADC_IN3 |
| PA4 | 7 | I/O | | Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK ⁽³⁾ , USART1_CK ⁽⁴⁾ , TIMER13_CH0, SPI1_NSS ⁽⁵⁾ Additional: ADC_IN4, CMP_IM4 |
| PA5 | 8 | I/O | | Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5, CMP_IM5 |
| PA6 | 9 | I/O | | Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, CMP_OUT Additional: ADC_IN6 |
| PA7 | 10 | I/O | | Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7 |
| PB1 | 11 | I/O | | Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK ⁽⁵⁾ Additional: ADC_IN9 |
| V _{SS} | 12 | P | | Default: V _{SS} |
| V _{DD} | 13 | P | | Default: V _{DD} |
| PA9 ⁽⁶⁾ | 14 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, I2C0_SCL, CK_OUT |
| PA10 ⁽⁶⁾ | 15 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA |
| PA13 | 16 | I/O | 5VT | Default: PA13 Alternate: SWDIO, IFRP_OUT, SPI1_MISO ⁽⁵⁾ |
| PA14 | 17 | I/O | 5VT | Default: PA14 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , SWCLK, SPI1_MOSI ⁽⁵⁾ |
| BOOT0 | 18 | I | | Default: BOOT0 |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32E230F4 devices only.
- (4) Functions are available on GD32E230F8/6 devices.
- (5) Functions are available on GD32E230F8 devices only.
- (6) Pin pair PA11/PA12 can be remapped instead of pin pair PA9/PA10 using SYSCFG_CFG0 register. [Table 2-10. Port A alternate functions summary](#) shows PA11/PA12 remap.

2.6.7 GD32E230xx pin alternate functions

Table 2-10. Port A alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|------------------------------|---|---------------|-----------|--------------------------|-------------------------------|--------------------------|---------|
| PA0 | | USART0_CTS ⁽¹⁾ /USART1_CTS ⁽²⁾ | | | I2C1_SCL ⁽³⁾ | | | CMP_OUT |
| PA1 | EVENTOUT | USART0_RTS ⁽¹⁾ /USART1_RTS ⁽²⁾ | | | I2C1_SDA ⁽³⁾ | TIMER14_CH0_ON ⁽³⁾ | | |
| PA2 | TIMER14_CH0 ⁽³⁾ | USART0_TX ⁽¹⁾ USART1_TX ⁽²⁾ | | | | | | |
| PA3 | TIMER14_CH1 ⁽³⁾ | USART0_RX ⁽¹⁾ USART1_RX ⁽²⁾ | | | | | | |
| PA4 | SPI0_NSS/I2S0_WS | USART0_CK ⁽¹⁾ USART1_CK ⁽²⁾ | | | TIMER13_CH0 | | SPI1_NSS ⁽³⁾ | |
| PA5 | SPI0_SCK/I2S0_CK | | | | | | | |
| PA6 | SPI0_MISO/I2S0_MCK | TIMER2_CH0 | TIMER0_BRKIN | | | TIMER15_CH0 | EVENT_OUT | CMP_OUT |
| PA7 | SPI0_MOSI/I2S0_SD | TIMER2_CH1 | TIMER0_CH0_ON | | TIMER13_CH0 | TIMER16_CH0 | EVENT_OUT | |
| PA8 | CK_OUT | USART0_CK | TIMER0_CH0 | EVENT_OUT | USART1_TX ⁽²⁾ | | | |
| PA9 | TIMER14_BRKIN ⁽³⁾ | USART0_TX | TIMER0_CH1 | | I2C0_SCL | | | |
| PA10 | TIMER16_BRKIN | USART0_RX | TIMER0_CH2 | | I2C0_SDA | | | |
| PA11 | EVENTOUT | USART0_CTS | TIMER0_CH3 | | I2C0_SMB_A | I2C1_SCL ⁽³⁾ | SPI1_IO2 ⁽³⁾ | CMP_OUT |
| PA12 | EVENTOUT | USART0_RTS | TIMER0_ETI | | I2C0_TXFRAME | I2C1_SDA ⁽³⁾ | SPI1_IO3 ⁽³⁾ | |
| PA13 | SWDIO | IFRP_OUT | | | | | SPI1_MISO ⁽³⁾ | |
| PA14 | SWCLK | USART0_TX ⁽¹⁾ USART1_TX ⁽²⁾ | | | | | SPI1_MOSI ⁽³⁾ | |
| PA15 | SPI0_NSS/I2S0_WS | USART0_RX ⁽¹⁾ USART1_RX ⁽²⁾ | | EVENT_OUT | | | SPI1_NSS ⁽³⁾ | |

Table 2-11. Port B alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|--|--|----------------|-------------------------------|--------------------------|-------------------------|-------------------------|-------------------------|
| PB0 | EVENTOUT | TIMER2_CH2 | TIMER0_CH1_ON | | USART1_RX ⁽²⁾ | | | |
| PB1 | TIMER13_CH0 | TIMER2_CH3 | TIMER0_CH2_ON | | | | SPI1_SCK ⁽³⁾ | |
| PB2 | | | TIMER2_ETI | | | | | |
| PB3 | SPI0_SCK/I2S0_SCK | EVENTOUT | | | | | | |
| PB4 | SPI0_MISO/I2S0_MCK | TIMER2_CH0 | EVENTOUT | | I2C0_TXFRAME | | TIMER16_BRKIN | |
| PB5 | SPI0_MOSI/I2S0_SD | TIMER2_CH1 | TIMER15_BRKIN | I2C0_SMBA | | | | |
| PB6 | USART0_TX | I2C0_SCL | TIMER15_CH0_ON | | | | | |
| PB7 | USART0_RX | I2C0_SDA | TIMER16_CH0_ON | | | | | |
| PB8 | | I2C0_SCL | TIMER15_CH0 | | | | | |
| PB9 | IFRP_OUT | I2C0_SDA | TIMER16_CH0 | EVENTOUT | | I2S0_MCK | | SPI1_NSS ⁽³⁾ |
| PB10 | | I2C0_SCL ⁽¹⁾ /I2C1_SCL ⁽³⁾ | | | | | SPI1_IO2 ⁽³⁾ | SPI1_SCK ⁽³⁾ |
| PB11 | EVENTOUT | I2C0_SDA ⁽¹⁾ /I2C1_SDA ⁽³⁾ | | | | | SPI1_IO3 ⁽³⁾ | |
| PB12 | SPI0_NSS ⁽¹⁾ /SPI1_NSS ⁽³⁾ | EVENTOUT | TIMER0_BRKIN | | I2C1_SMBA ⁽³⁾ | | | |
| PB13 | SPI0_SCK ⁽¹⁾ /SPI1_SCK ⁽³⁾ | I2C1_TXFRAME ⁽³⁾ | TIMER0_CH0_ON | | | I2C1_SCL ⁽³⁾ | | |
| PB14 | SPI0_MISO ⁽¹⁾ /SPI1_MISO ⁽³⁾ | TIMER14_CH0 ⁽³⁾ | TIMER0_CH1_ON | | | I2C1_SDA ⁽³⁾ | | |
| PB15 | SPI0_MOSI ⁽¹⁾ /SPI1_MOSI ⁽³⁾ | TIMER14_CH1 ⁽³⁾ | TIMER0_CH2_ON | TIMER14_CH0_ON ⁽³⁾ | | | | |

Table 2-12. Port F alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 |
|----------|-------------------------|----------|-----|-----|-----|-----|-----|
| PF0 | | I2C0_SDA | | | | | |
| PF1 | | I2C0_SCL | | | | | |
| PF6 | I2C0_SCL ⁽¹⁾ | | | | | | |

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 |
|----------|---|-----|-----|-----|-----|-----|-----|
| | ¹ /I2C1_SCL (3) | | | | | | |
| PF7 | I2C0_SDA ¹ ¹ /I2C1_SDA A ⁽³⁾ | | | | | | |

Notes:

- (1) Functions are available on GD32E230x4 devices only.
- (2) Functions are available on GD32E230x8/6 devices.
- (3) Functions are available on GD32E230x8 devices only.

3 Functional description

3.1 ARM® Cortex®-M23 core

The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M23 processor core

- Up to 72 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Ultra-low power, energy-efficient operation
- Excellent code density
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M23 processor is based on the ARMv8-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M23:

- Internal Bus Matrix connected with AHB master, Serial Wire Debug Port and Single-cycle IO port
- Nested Vectored Interrupt Controller (NVIC)
- Breakpoint Unit(BPU)
- Data Watchpoint and Trace (DWT)
- Serial Wire JTAG Debug Port (SWJ-DP)

3.2 Embedded memory

- Up to 64 Kbytes of Flash memory
- Up to 8 Kbytes of SRAM with hardware parity checking

64 Kbytes of inner Flash and 8 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with 0~2 wait states. [Table 2-3.](#)

[GD32E230xx memory map](#) shows the memory map of the GD32E230xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator

- Internal 28 MHz RC oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 1.8 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 72 MHz/72 MHz/72 MHz. See [Figure 2-8. GD32E230xx clock tree](#) for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.8 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , V_{DDA} range: 1.8 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- V_{BAK} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PA14 and PA15).

3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance

between the CPU operating time, speed and power consumption.

■ **Sleep mode**

In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

■ **Deep-sleep mode**

In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC tamper and timestamp, CMP output, LVD output and USART wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

■ **Standby mode**

In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{SSA} to V_{DDA}
- Temperature sensor

One 12-bit 2 MSPS multi-channel ADC is integrated in the device. It has a total of 12 multiplexed channels: up to 10 external channels, 1 channel for internal temperature sensor (V_{SENSE}) and 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between V_{SSA} and V_{DDA} . An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced timer (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7 DMA

- 5 channels DMA controller
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs and I2S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.8 General-purpose inputs/outputs (GPIOs)

- Up to 39 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 39 general purpose I/O pins (GPIO) in GD32E230xx, named PA0 ~ PA15 and PB0 ~ PB15, PC13 ~ PC15, PF0 ~ PF1, PF6 ~ PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull open-drain or analog), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.9 Timers and PWM generation

- One 16-bit advanced timer (TIMER0), up to five 16-bit general timers (TIMER2, TIMER13 ~ TIMER16), and one 16-bit basic timer (TIMER5)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels.

It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center- aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMExx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER2 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIMER13 ~ TIMER16 is based on a 16-bit auto-reload up counter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 can also be used as a simple 16-bit time base.

The GD32E230xx have two watchdog peripherals, free watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.10 Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers.
- Calendar with subsecond, second, minute, hour, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 0.954 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

3.11 Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- Supports SAM_V mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.12 Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Separate transmit and receive 32-bit FIFO with DMA capability (only in SPI1)
- Data frame size can be 4 to 16 bits (only in SPI1)
- Quad-SPI configuration available in master mode (only in SPI1)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Specially, SPI1 has separate transmit and receive 32-bit FIFO with DMA capability and its data frame size can be 4 to 16 bits. Quad-SPI master mode is also supported in SPI1.

3.13 Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating frequency up to 4.5 MBits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.14 Inter-IC sound (I2S)

- One I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz, multiplexed with SPI0
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32E230xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI0. The audio sampling frequency from 8 KHz to 192 KHz is supported with less than 0.5% accuracy error.

3.15 Comparators (CMP)

- One fast rail-to-rail low-power comparators with software configurable
- Programmable reference voltage (internal or external I/O)

One Comparator (CMP) is implemented within the devices. It can wake up from deep-sleep mode to generate interrupts and breaks for the timers and also can be combined as a window comparator. The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

3.16 Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.17 Package and operation temperature

- LQFP48 (GD32E230CxTx), LQFP32 (GD32E230KxTx), QFN32 (GD32E230KxUx), QFN28 (GD32E230GxUx), TSSOP20 (GD32E230FxPx) and LGA20 (GD32E230FvVx).
- Operation temperature range: -40°C to +85°C (industrial level)

4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings

| Symbol | Parameter | Min | Max | Unit |
|----------------------|--|-----------------|-----------------|------|
| V_{DD} | External voltage range ⁽¹⁾ | $V_{SS} - 0.3$ | $V_{SS} + 3.6$ | V |
| V_{DDA} | External analog supply voltage | $V_{SSA} - 0.3$ | $V_{SSA} + 3.6$ | V |
| V_{IN} | Input voltage on 5V tolerant pin ⁽²⁾ | $V_{SS} - 0.3$ | $V_{DD} + 4.0$ | V |
| | Input voltage on other I/O | $V_{SS} - 0.3$ | 4.0 | V |
| $ \Delta V_{DDx} $ | Variations between different V_{DD} power pins | — | 50 | mV |
| $ V_{SSx} - V_{SS} $ | Variations between different ground pins | — | 50 | mV |
| I_{IO} | Maximum current for GPIO pins | — | 25 | mA |
| I_{INJ} | Injected current on 5V tolerant pin | — | ± 5 | mA |
| | Injected current on other I/O | — | ± 5 | mA |
| ΣI_{INJ} | Injected current on all I/O ⁽³⁾ | — | ± 25 | mA |
| T_A | Operating temperature range | -40 | +85 | °C |
| T_{STG} | Storage temperature range | -55 | +150 | °C |
| T_J | Maximum junction temperature | — | 125 | °C |

(1) All main power and ground pins should be connected to an external power source within the allowable range.

(2) V_{IN} maximum value cannot exceed 6.5V and it must be below the maximum allowable injection current value refer to [Table 4-1. Absolute maximum ratings](#)

(3) The maximum $\Sigma I_{INJ}(PIN)$ is the absolute sum of the negative and positive injection currents (instantaneous values).

4.2 Operating conditions characteristics

Table 4-2. DC operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------------------------|------------|-----|-----|-----|------|
| V_{DD} | Supply voltage | — | 1.8 | 3.3 | 3.6 | V |
| V_{DDA} | Analog supply voltage ADC not used | — | 1.8 | 3.3 | 3.6 | V |
| | Analog supply voltage ADC used | | 2.4 | 3.3 | 3.6 | |

Table 4-3. Clock frequency

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------|----------------------|------------|-----|-----|------|
| f _{HCLK} | AHB clock frequency | — | 0 | 72 | MHz |
| f _{APB1} | APB1 clock frequency | — | 0 | 72 | MHz |
| f _{APB2} | APB2 clock frequency | — | 0 | 72 | MHz |

Table 4-4. Operating conditions at Power up/ Power down

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|--------------------------------|------------|-----|-----|------|
| t _{VDD} | V _{DD} rise time rate | | 0 | ∞ | us/V |
| | V _{DD} fall time rate | | 20 | ∞ | |

Table 4-5. Start-up timings of Operating conditions

| Symbol | Parameter | Conditions | Typ | Unit |
|--------------------------------------|---------------|-------------------------|-----|------|
| t _{start-up} ⁽¹⁾ | Start-up time | Clock source from HXTAL | 432 | us |
| | | Clock source from IRC8M | 76 | |

(1). After power-up, the start-up time is the time between the rising edge of NRST high and the main function.

Table 4-6. Power saving mode wakeup timings characteristics

| Symbol | Parameter | Typ | Unit |
|--|---|------|------|
| t _{Sleep} ⁽¹⁾ | Wakeup from Sleep mode | 3.5 | μs |
| t _{Deep-sleep} ⁽¹⁾ | Wakeup from Deep-sleep mode (LDO On) | 17.1 | |
| | Wakeup from Deep-sleep mode (LDO in low power mode) | 17.1 | |
| t _{Standby} ⁽¹⁾ | Wakeup from Standby mode | 77.5 | |

(1).The wakeup times is measured from the wakeup event to the point at which the application code reads the first instruction under the the below conditions:

V_{DD}=V_{DDA}=3.3V, IRC8M=System clock=8MHz.

4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from embedded Flash with the following specifications.

Table 4-7. Power consumption characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|---|-----|-----|-----|------|
| I _{DD} | Supply current (Run mode) | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock=72 MHz, All peripherals enabled | — | 8.5 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock =72 MHz, All peripherals disabled | — | 5.4 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock=48 MHz, All peripherals enabled | — | 6.2 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock =48 MHz, All peripherals disabled | — | 4.2 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock=36 MHz, All peripherals enabled | — | 5.1 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock =36 MHz, All peripherals disabled | — | 3.6 | — | mA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------------------------|--|-----|-----|-----|------|
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock=24 MHz, All peripherals enabled | — | 4.0 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock =24 MHz, All peripherals disabled | — | 2.9 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock=16 MHz, All peripherals enabled | — | 3.2 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock =16 MHz, All peripherals disabled | — | 2.5 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock=8 MHz, All peripherals enabled | — | 2.4 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock =8 MHz, All peripherals disabled | — | 2.1 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock=4 MHz, All peripherals enabled | — | 0.8 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock =4 MHz, All peripherals disabled | — | 0.6 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock=2 MHz, All peripherals enabled | — | 0.6 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock =2 MHz, All peripherals disabled | — | 0.5 | — | mA |
| | Supply current (Sleep mode) | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =72 MHz, All peripherals enabled | — | 7.4 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =72 MHz, All peripherals disabled | — | 3.7 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals enabled | — | 5.5 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals disabled | — | 3.1 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =36 MHz, All peripherals enabled | — | 4.5 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =36 MHz, All peripherals disabled | — | 2.7 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =24 MHz, All peripherals enabled | — | 3.6 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =24 MHz, All peripherals disabled | — | 2.4 | — | mA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|----------------------------------|--|-----|------|-----|------|
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =16 MHz, All peripherals enabled | — | 3.0 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =16 MHz, All peripherals disabled | — | 2.1 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =8 MHz, All peripherals enabled | — | 2.3 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =8 MHz, All peripherals disabled | — | 1.9 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =4 MHz, All peripherals enabled | — | 0.7 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =4 MHz, All peripherals disabled | — | 0.5 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =2 MHz, All peripherals enabled | — | 0.5 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =2 MHz, All peripherals disabled | — | 0.4 | — | mA |
| | Supply current (Deep-sleep mode) | V _{DD} =V _{DDA} =3.3V, LDO in run mode, IRC40K off, RTC off, All GPIOs analog mode | — | 25.5 | — | μA |
| | | V _{DD} =V _{DDA} =3.3V, LDO in low power mode, IRC40K off, RTC off, All GPIOs analog mode | — | 12.3 | — | μA |
| | Supply current (Standby mode) | V _{DD} =V _{DDA} =3.3V, LXTAL off, IRC40K on, RTC on | — | 3.8 | — | μA |
| | | V _{DD} =V _{DDA} =3.3V, LXTAL off, IRC40K on, RTC off | — | 3.6 | — | μA |
| | | V _{DD} =V _{DDA} =3.3V, LXTAL off, IRC40K off, RTC off, VDDA Monitor on | — | 3.1 | — | μA |
| | | V _{DD} =V _{DDA} =3.3V, LXTAL off, IRC40K off, RTC off, VDDA Monitor off | — | 1.6 | — | μA |
| I _{LXTAL+RTC} | LXTAL+RTC current | V _{DD} =V _{DDA} =3.6 V, LXTAL on with external crystal, RTC on, Higher driving | — | 1.43 | — | μA |
| | | V _{DD} =V _{DDA} =3.3 V, LXTAL on with external crystal, RTC on, Higher driving | — | 1.36 | — | μA |
| | | V _{DD} =V _{DDA} =2.5 V, LXTAL on with external crystal, RTC on, Higher driving | — | 1.23 | — | μA |
| | | V _{DD} =V _{DDA} =1.8 V, LXTAL on with external | — | 1.15 | — | μA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|---|-----|------|-----|------|
| | | crystal, RTC on, Higher driving | | | | |
| | | V _{DD} =V _{DDA} =3.6 V, LXTAL on with external crystal, RTC on, Medium High driving | — | 1.13 | — | μA |
| | | V _{DD} =V _{DDA} =3.3 V, LXTAL on with external crystal, RTC on, Medium High driving | — | 1.06 | — | μA |
| | | V _{DD} =V _{DDA} =2.5 V, LXTAL on with external crystal, RTC on, Medium High driving | — | 0.95 | — | μA |
| | | V _{DD} =V _{DDA} =1.8 V, LXTAL on with external crystal, RTC on, Medium High driving | — | 0.86 | — | μA |
| | | V _{DD} =V _{DDA} =3.6 V, LXTAL on with external crystal, RTC on, Medium Low driving | — | 0.84 | — | μA |
| | | V _{DD} =V _{DDA} =3.3 V, LXTAL on with external crystal, RTC on, Medium Low driving | — | 0.76 | — | μA |
| | | V _{DD} =V _{DDA} =2.5 V, LXTAL on with external crystal, RTC on, Medium Low driving | — | 0.64 | — | μA |
| | | V _{DD} =V _{DDA} =1.8 V, LXTAL on with external crystal, RTC on, Medium Low driving | — | 0.56 | — | μA |
| | | V _{DD} =V _{DDA} =3.6 V, LXTAL on with external crystal, RTC on, Low driving | — | 0.74 | — | μA |
| | | V _{DD} =V _{DDA} =3.3 V, LXTAL on with external crystal, RTC on, Low driving | — | 0.67 | — | μA |
| | | V _{DD} =V _{DDA} =2.5 V, LXTAL on with external crystal, RTC on, Low driving | — | 0.56 | — | μA |
| | | V _{DD} =V _{DDA} =1.8 V, LXTAL on with external crystal, RTC on, Low driving | — | 0.47 | — | μA |

Notes:

(1) When System Clock is less than 4MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(2) When System Clock is greater than 8MHz, a crystal 8MHz is used, and the HXTAL bypass function is closed, using PLL.

(3) When analog peripheral blocks such as ADCs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered

The power measurements specified in the tables represent that code with data executing from embedded Flash with the following specifications.

Table 4-8. Peripheral current consumption characteristics

| Peripherals ⁽¹⁾ | | Typical consumption at 25°C (TYP) | Unit |
|----------------------------|--------|--------------------------------------|------|
| APB1 | PMU | 1.44 | mA |
| | I2C1 | 1.38 | |
| | I2C0 | 1.38 | |
| | USART1 | 1.34 | |
| | SPI1 | 1.37 | |
| | WWDGT | 1.32 | |

| Peripherals ⁽¹⁾ | | Typical consumption at 25°C (TYP) | Unit |
|----------------------------|--------------------------|--------------------------------------|------|
| | TIMER13 | 1.36 | |
| | TIMER5 | 0.17 | |
| | TIMER2 | 0.23 | |
| APB2 | DBGMCU | 1.3 | |
| | TIMER16 | 1.42 | |
| | TIMER15 | 1.42 | |
| | TIMER14 | 1.49 | |
| | USART0 | 1.63 | |
| | SPI0 | 1.38 | |
| | TIMER0 | 1.68 | |
| | ADC ⁽²⁾ | 0.95 | |
| | CFG & CMP ⁽³⁾ | 1.27 | |
| AHB | GPIOF | 1.31 | |
| | GPIOC | 1.31 | |
| | GPIOB | 1.34 | |
| | GPIOA | 1.34 | |
| | CRC | 0.16 | |
| | DMA | 0.15 | |

(1) Conditions: $V_{DD} = V_{DDA} = 3.3V$, IRC8M = 8MHz, system clock = $f_{HCLK} = 72MHz$, $f_{APB1} = f_{APB2} = f_{HCLK}$.

(2) ADC: $f_{ADCCLK} = IRC28M$, ADCON bit set to 1 in ADC_CTL1.

(3) CMP: CMP enabled by setting CMPEN bit in CMP_CS. CMP mode set to High Speed.

4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in [Table 4-9. EMS characteristics](#), based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-9. EMS characteristics

| Symbol | Parameter | Conditions | Level/Class |
|-----------|--|--|-------------|
| V_{ESD} | Voltage applied to all device pins to induce a functional disturbance | $V_{DD} = 3.3V$, $T_A = +25^\circ C$, LQFP48, $f_{HCLK} = 72MHz$ conforms to IEC 61000-4-2 | 3A |
| V_{FTB} | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins | $V_{DD} = 3.3V$, $T_A = +25^\circ C$, LQFP48, $f_{HCLK} = 72MHz$ conforms to IEC 61000-4-4 | 4A |

EMI (Electromagnetic Interference) emission testing result is given in [Table 4-10. EMI characteristics](#) compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 4-10. EMI characteristics

| Symbol | Parameter | Conditions | Tested frequency band | Conditions | | Unit |
|------------------|------------|---|-----------------------|------------|-----|------|
| | | | | 48M | 72M | |
| S _{EMI} | Peak level | V _{DD} = 3.3 V, T _A = +25 °C, compliant with IEC 61967-2 | 0.1 to 2 MHz | — | — | dBμV |
| | | | 2 to 30 MHz | — | — | |
| | | | 30 to 130 MHz | — | — | |
| | | | 130 MHz to 1GHz | — | — | |

4.5 Power supply supervisor characteristics

Table 4-11. Power supply supervisor characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|-----------------------------------|-----------------------------|-----|------|-----|------|
| V _{LVD} | Low Voltage Detector Threshold | LVDT[2:0]=000, rising edge | — | 2.11 | — | V |
| | | LVDT[2:0]=000, falling edge | — | 2.01 | — | V |
| | | LVDT[2:0]=001, rising edge | — | 2.25 | — | V |
| | | LVDT[2:0]=001, falling edge | — | 2.16 | — | V |
| | | LVDT[2:0]=010, rising edge | — | 2.39 | — | V |
| | | LVDT[2:0]=010, falling edge | — | 2.29 | — | V |
| | | LVDT[2:0]=011, rising edge | — | 2.52 | — | V |
| | | LVDT[2:0]=011, falling edge | — | 2.43 | — | V |
| | | LVDT[2:0]=100, rising edge | — | 2.66 | — | V |
| | | LVDT[2:0]=100, falling edge | — | 2.57 | — | V |
| | | LVDT[2:0]=101, rising edge | — | 2.80 | — | V |
| | | LVDT[2:0]=101, falling edge | — | 2.71 | — | V |
| | | LVDT[2:0]=110, rising edge | — | 2.95 | — | V |
| | | LVDT[2:0]=110, falling edge | — | 2.84 | — | V |
| | | LVDT[2:0]=111, rising edge | — | 3.08 | — | V |
| LVDT[2:0]=111, falling edge | — | 2.98 | — | V | | |
| V _{LVDhyst} ⁽¹⁾ | LVD hysteresis | — | — | 100 | — | mV |
| V _{POR} | Power on reset threshold | Rising edge | — | 1.71 | — | V |
| V _{PDR} | Power down reset threshold | Falling edge | — | 1.67 | — | V |
| V _{PDRhyst} ⁽¹⁾ | PDR hysteresis | — | — | 40 | — | mV |
| t _{RSTTEMP} | Reset temporization | — | — | 2.5 | — | ms |

(1) Based on design, not actual test values.

4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up

(LU) test is based on the two measurement methods.

Table 4-12. ESD characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|--|-----|-----|------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A=25\text{ }^\circ\text{C}$; JESD22-A114 | — | — | 6000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A=25\text{ }^\circ\text{C}$; JESD22-C101 | — | — | 2000 | V |

Table 4-13. Static latch-up characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|----------------------------------|---|-----|-----|-----------|------|
| LU | I-test | $T_A=25\text{ }^\circ\text{C}$; JESD78 | — | — | ± 200 | mA |
| | V_{supply} over voltage | | — | — | 5.4 | V |

4.7 External clock characteristics

Table 4-14. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|--|---|-----|-----|-----|------------|
| f_{HXTAL} | Crystal or ceramic frequency ⁽¹⁾ | $V_{DD}=3.3\text{V}$ | 4 | 8 | 32 | MHz |
| R_F | Feedback resistor | $V_{DD}=3.3\text{V}$ | — | — | — | k Ω |
| C_{HXTAL} | Recommended matching capacitance on OSCIN and OSCOUT | — | — | 20 | 30 | pF |
| $I_{DD}(\text{HXTAL})$ | Crystal or ceramic operating current | $V_{DD}=3.3\text{V}$, $T_A=25\text{ }^\circ\text{C}$ | — | 1.0 | — | mA |
| $g_m(\text{HXTAL})$ | Crystal or ceramic transconductance | Startup | — | — | — | mA/V |
| t_s | Crystal or ceramic startup time | $V_{DD}=3.3\text{V}$, $T_A=25\text{ }^\circ\text{C}$ | — | 2 | — | ms |

(1) Based on design, not actual test values.

Note: $C_{\text{HXTAL1}} = C_{\text{HXTAL2}} = 2 \cdot (C_{\text{LOAD}} - C_s)$, For C_{HXTAL1} and C_{HXTAL2} , it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD} , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_s , it is PCB and MCU pin stray capacitance (Typ. $C_s = 10\text{pf}$).

Table 4-15. High speed external user clock characteristics (HXTAL in bypass mode)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|---|----------------------|-------------|-----|-------------|------|
| $f_{\text{HXTAL_ext}}$ | External clock source or oscillator frequency | $V_{DD}=3.3\text{V}$ | 1 | 8 | 50 | MHz |
| V_{HXTALH} | OSCIN input pin high level voltage | $V_{DD}=3.3\text{V}$ | $0.7V_{DD}$ | — | V_{DD} | V |
| V_{HXTALL} | OSCIN input pin low level voltage | | V_{SS} | — | $0.3V_{DD}$ | |
| $t_{H/L}(\text{HXTAL})^{(1)}$ | OSCIN high or low time | — | 5 | — | — | ns |
| $t_{R/F}(\text{HXTAL})^{(1)}$ | OSCIN rise or fall time | — | — | — | 10 | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|-------------------------|------------|-----|-----|-----|------|
| $C_{IN}^{(1)}$ | OSCIN input capacitance | — | — | 5 | — | pF |
| DuCy(HXTAL) | Duty cycle | — | 30 | 50 | 70 | % |

(1) Based on design, not actual test values.

Table 4-16. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|--|-----------------------------------|-----|--------|-----|-----------|
| $f_{LXTAL}^{(1)}$ | Crystal or ceramic frequency | $V_{DD}=3.3V$ | — | 32.768 | — | KHz |
| R_F | Feedback resistor | $V_{DD}=3.3V$ | — | — | — | $M\Omega$ |
| $C_{LXTAL}^{(1)}$ | Recommended matching capacitance on OSC32IN and OSC32OUT | — | — | — | 15 | pF |
| $I_{DD}(LXTAL)$ | Crystal or ceramic operating current | $V_{DD}=3.3V$, High Drive | — | 1.2 | — | μA |
| | | $V_{DD}=3.3V$, Medium High Drive | — | 1.0 | — | |
| | | $V_{DD}=3.3V$, Medium Low Drive | — | 0.6 | — | |
| | | $V_{DD}=3.3V$, Low Drive | — | 0.5 | — | |
| $g_m(LXTAL)$ | Crystal or ceramic transconductance | Startup | — | — | — | $\mu A/V$ |
| $t_{SULXTAL}$ | Crystal or ceramic startup time | $V_{DD}=3.3V$ | — | 2 | — | s |

(1) Based on design, not actual test values.

Note: $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_s)$, For C_{LXTAL1} and C_{LXTAL2} , it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD} , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_s , it is PCB and MCU pin stray capacitance (Typ. $C_s = 2pf \sim 7pf$).

Table 4-17. Low speed external user clock characteristics (LXTAL in bypass mode)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|---------------|--------|---------|--------|------|
| $f_{LXTAL_ext}^{(1)}$ | External clock source or oscillator frequency | $V_{DD}=3.3V$ | — | 32.768. | 1000 | kHz |
| V_{LXTALH} | OSC32IN input pin high level voltage | $V_{DD}=3.3V$ | 0.7VDD | — | VDD | V |
| V_{LXTALL} | OSC32IN input pin low level voltage | | VSS | — | 0.3VDD | |
| $t_{H/L}(LXTAL)^{(1)}$ | OSC32IN high or low time | — | 450 | — | — | ns |
| $t_{R/F}(LXTAL)^{(1)}$ | OSC32IN rise or fall time | — | — | — | 50 | |
| $C_{IN}^{(1)}$ | OSC32IN input capacitance | — | — | 5 | — | pF |
| DuCy(LXTAL) | Duty cycle | — | 30 | 50 | 70 | % |

(1) Based on design, not actual test values.

4.8 Internal clock characteristics

Table 4-18. High speed internal clock (IRC8M) characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|--|------|-----|------|---------|
| f_{IRC8M} | High Speed Internal Oscillator (IRC8M) frequency | $V_{DD}=3.3V$ | — | 8 | — | MHz |
| ACC_{IRC8M} | IRC8M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}=3.3V, T_A=-40^{\circ}C \sim +105^{\circ}C^{(2)}$ | -4.0 | — | +5.0 | % |
| | | $V_{DD}=3.3V, T_A=0^{\circ}C \sim +85^{\circ}C^{(2)}$ | -2.0 | — | +2.0 | % |
| | | $V_{DD}=3.3V, T_A=25^{\circ}C$ | -1.0 | — | +1.0 | % |
| | IRC8M oscillator Frequency accuracy, User trimming step | — | — | 0.5 | — | % |
| D_{IRC8M} | IRC8M oscillator duty cycle | $V_{DD}=3.3V, f_{IRC8M}=8MHz$ | 45 | 50 | 55 | % |
| $I_{DDIRC8M}$ | IRC8M oscillator operating current | $V_{DD}=3.3V, f_{IRC8M}=8MHz$ | — | 55 | 80 | μA |
| $t_{SUIRC8M}^{(3)}$ | IRC8M oscillator startup time | $V_{DD}=3.3V, f_{IRC8M}=8MHz$ | — | 1.5 | 2 | us |

(1) $V_{DD} = 3.3 V$, $T_A = -40$ to $105^{\circ}C$ unless otherwise specified.

(2) Based on characterization, not actual test values.

(3) Based on design, not actual test values.

Table 4-19. High speed internal clock (IRC28M) characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|--|--|------|-----|------|---------|
| f_{IRC28M} | High Speed Internal Oscillator (IRC28M) frequency | $V_{DD}=3.3V$ | — | 28 | — | MHz |
| ACC_{IRC28M} | IRC28M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}=3.3V, T_A=-40^{\circ}C \sim +105^{\circ}C^{(2)}$ | -4.0 | — | +5.0 | % |
| | | $V_{DD}=3.3V, T_A=0^{\circ}C \sim +85^{\circ}C^{(2)}$ | -3.0 | — | +3.0 | % |
| | | $V_{DD}=3.3V, T_A=25^{\circ}C$ | -2.0 | — | +2.0 | % |
| | IRC28M oscillator Frequency accuracy, User trimming step | — | — | 0.5 | — | % |
| D_{IRC28M} | IRC28M oscillator duty cycle | $V_{DD}=3.3V, f_{IRC28M}=16MHz$ | 45 | 50 | 55 | % |
| $I_{DDIRC28M}$ | IRC28M oscillator operating current | $V_{DD}=3.3V, f_{IRC28M}=16MHz$ | — | 140 | 200 | μA |
| $t_{SUIRC28M}^{(3)}$ | IRC28M oscillator startup time | $V_{DD}=3.3V, f_{IRC28M}=16MHz$ | — | 1.5 | 2 | μs |

(1) $V_{DD} = 3.3 V$, $T_A = -40$ to $105^{\circ}C$ unless otherwise specified.

(2) Based on characterization, not actual test values.

(3) Based on design, not actual test values.

Table 4-20. Low speed internal clock (IRC40K) characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|--|--|-----|------|-----|------|
| $f_{IRC40K}^{(2)}$ | Low Speed Internal oscillator (IRC40K) frequency | $V_{DD}=V_{DDA}=3.3V,$ $T_A=-40^{\circ}C \sim +85^{\circ}C$ | 30 | 38.5 | 60 | KHz |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|-------------------------------------|--|-----|------|-----|---------|
| $I_{DDIRC40K}^{(3)}$ | IRC40K oscillator operating current | $V_{DD}=V_{DDA}=3.3V, T_A=25^{\circ}C$ | — | 0.41 | — | μA |
| $t_{SUIRC40K}^{(3)}$ | IRC40K oscillator startup time | $V_{DD}=V_{DDA}=3.3V, T_A=25^{\circ}C$ | — | 33 | — | μs |

(1). $V_{DD} = 3.3 V$, $T_A = -40$ to $105^{\circ}C$ unless otherwise stated.

(2). Based on characterization, not actual test values.

(3). Based on design, not actual test values.

4.9 PLL characteristics

Table 4-21. PLL characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|---------------------------------|----------------|------------------|-----|-----|---------|
| f_{PLLIN} | PLL input clock frequency | — | 1 ⁽¹⁾ | — | 25 | MHz |
| f_{PLLOUT} | PLL output clock frequency | — | 16 | — | 72 | MHz |
| t_{LOCK} | PLL lock time | — | — | — | 300 | μs |
| $I_{DD}^{(2)}$ | Current consumption on V_{DD} | VCO freq=72MHz | — | 130 | — | μA |
| Jitter $_{PLL}^{(3)}$ | Cycle to cycle Jitter | System clock | — | 300 | — | ps |

(1) Based on design, not actual test values.

(2) Based on characterization, not actual test values.

(3) Value given with main PLL running.

4.10 Memory characteristics

Table 4-22. Flash memory characteristics

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max ⁽¹⁾ | Unit |
|--------------|---|--------------------------------------|--------------------|-----|--------------------|---------|
| PE $_{CYC}$ | Number of guaranteed program /erase cycles before failure (Endurance) | $T_A=-40^{\circ}C \sim +85^{\circ}C$ | 100 | — | — | kcycles |
| t_{RET} | Data retention time | 10k cycles at $T_A=85^{\circ}C$ | 10 | — | — | years |
| t_{PROG} | Word programming time | $T_A=-40^{\circ}C \sim +85^{\circ}C$ | 37 | — | 42 | μs |
| t_{ERASE} | Page erase time | $T_A=-40^{\circ}C \sim +85^{\circ}C$ | 0.8 | — | 1.1 | ms |
| t_{MERASE} | Mass erase time | $T_A=-40^{\circ}C \sim +85^{\circ}C$ | 3.2 | — | 4 | ms |

(1) Based on characterization, not actual test values.

4.11 NRST pin characteristics

Table 4-23. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|------------------------------|-----------------------|------|-----|------|------|
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | $V_{DD}=V_{DDA}=1.8V$ | -0.5 | — | 0.71 | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|------------------------------------|-----------------------|------|------|--------------|------------|
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | 1.08 | — | $V_{DD}+0.5$ | |
| V_{hyst} | Schmidt trigger Voltage hysteresis | | — | 370 | — | |
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | $V_{DD}=V_{DDA}=2.5V$ | -0.5 | — | 1.05 | V |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | 1.42 | — | $V_{DD}+0.5$ | |
| V_{hyst} | Schmidt trigger Voltage hysteresis | | — | 370 | — | mV |
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | $V_{DD}=V_{DDA}=3.3V$ | -0.5 | — | 1.4 | V |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | 1.8 | — | $V_{DD}+0.5$ | |
| V_{hyst} | Schmidt trigger Voltage hysteresis | | — | 400 | — | mV |
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | $V_{DD}=V_{DDA}=3.6V$ | -0.5 | — | 1.53 | V |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | 1.95 | — | $V_{DD}+0.5$ | |
| V_{hyst} | Schmidt trigger Voltage hysteresis | | — | 420 | — | mV |
| $R_{pu}^{(2)}$ | Pull-up equivalent resistor | — | — | 40.3 | — | K Ω |

(1).Based on design, not actual test values.

(2).Based on characterization, not actual test values.

4.12 GPIO characteristics

Table 4-24. I/O port DC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--|---------------|----------|-----|----------|------|
| V_{IL} | Standard IO Low level input voltage | $V_{DD}=1.8V$ | V_{SS} | — | 0.80 | V |
| | | $V_{DD}=2.5V$ | | — | 1.10 | |
| | | $V_{DD}=3.3V$ | | — | 1.40 | |
| | | $V_{DD}=3.6V$ | | — | 1.60 | |
| V_{IL} | 5V-tolerant IO Low level input voltage | $V_{DD}=1.8V$ | V_{SS} | — | 0.80 | V |
| | | $V_{DD}=2.5V$ | | — | 1.10 | |
| | | $V_{DD}=3.3V$ | | — | 1.40 | |
| | | $V_{DD}=3.6V$ | | — | 1.60 | |
| V_{IH} | Standard IO High level input voltage | $V_{DD}=1.8V$ | 1.10 | — | V_{DD} | V |
| | | $V_{DD}=2.5V$ | 1.50 | — | | |
| | | $V_{DD}=3.3V$ | 1.90 | — | | |
| | | $V_{DD}=3.6V$ | 2.00 | — | | |
| V_{IH} | 5V-tolerant IO High level input voltage | $V_{DD}=1.8V$ | 1.10 | — | V_{DD} | V |
| | | $V_{DD}=2.5V$ | 1.50 | — | | |
| | | $V_{DD}=3.3V$ | 1.90 | — | | |
| | | $V_{DD}=3.6V$ | 2.00 | — | | |
| V_{OL} | Low level output voltage for an IO Pin ($I_{IO} = +8mA$) | $V_{DD}=1.8V$ | — | — | 0.20 | V |
| | | $V_{DD}=2.5V$ | — | — | 0.20 | |
| | | $V_{DD}=3.3V$ | — | — | 0.10 | |
| | | $V_{DD}=3.6V$ | — | — | 0.10 | |
| V_{OL} | Low level output voltage for an IO Pin | $V_{DD}=1.8V$ | — | — | — | V |
| | | $V_{DD}=2.5V$ | — | — | 0.50 | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---|-----------------------|------|-----|------|------|
| | (I _{IO} = +20mA) | V _{DD} =3.3V | — | — | 0.40 | |
| | | V _{DD} =3.6V | — | — | 0.40 | |
| V _{OH} | High level output voltage for an IO Pin (I _{IO} = +8mA) | V _{DD} =1.8V | 1.50 | — | — | V |
| | | V _{DD} =2.5V | 2.30 | — | — | |
| | | V _{DD} =3.3V | 3.10 | — | — | |
| | | V _{DD} =3.6V | 3.40 | — | — | |
| V _{OH} | High level output voltage for an IO Pin (I _{IO} = +20mA) | V _{DD} =1.8V | — | — | — | V |
| | | V _{DD} =2.5V | 1.90 | — | — | |
| | | V _{DD} =3.3V | 2.80 | — | — | |
| | | V _{DD} =3.6V | 3.10 | — | — | |
| R _{PU} | Internal pull-up resistor | — | — | 40 | — | kΩ |
| R _{PD} | Internal pull-down resistor | — | — | 40 | — | kΩ |

Table 4-25. I/O port AC characteristics^{(1) (2)}

| GPIOx_OSPD[1:0] bit value | Parameter | Conditions | Typ | Max | Unit |
|--|---|---|-----------|-----------|------|
| GPIOx_OSPD0->OSPDy[1:0] =X0 (IO_Speed = 2MHz) | Maximum frequency ⁽³⁾ | V _{DD} =1.8V, C _L =10pF | 2 | 10 | MHz |
| | | V _{DD} =1.8V, C _L =30pF | 2 | 8 | |
| | | V _{DD} =1.8V, C _L =50pF | 2 | 6 | |
| | Output high/ low to low/ high level fall/ rise time | V _{DD} =1.8V, C _L =10pF | 24.4/23.4 | 29.4/33.4 | ns |
| | | V _{DD} =1.8V, C _L =30pF | 31.6/29.8 | 37.6/36.8 | |
| | | V _{DD} =1.8V, C _L =50pF | 49/43.2 | 51/42.2 | |
| GPIOx_OSPD0->OSPDy[1:0] =01 (IO_Speed = 10MHz) | Maximum frequency ⁽³⁾ | V _{DD} =1.8V, C _L =10pF | 10 | 32 | MHz |
| | | V _{DD} =1.8V, C _L =30pF | 10 | 26 | |
| | | V _{DD} =1.8V, C _L =50pF | 10 | 18 | |
| | Output high/ low to low/ high level fall/ rise time | V _{DD} =1.8V, C _L =10pF | 8.8/9.2 | 10.0/10.2 | ns |
| | | V _{DD} =1.8V, C _L =30pF | 12.0/12.8 | 12.0/11.0 | |
| | | V _{DD} =1.8V, C _L =50pF | 15/13.6 | 17.2/15.8 | |
| GPIOx_OSPD0->OSPDy[1:0] =11 (IO_Speed = 50MHz) | Maximum frequency ⁽³⁾ | V _{DD} =1.8V, C _L =10pF | — | 20 | MHz |
| | | V _{DD} =1.8V, C _L =30pF | 50 | 54 | |
| | | V _{DD} =1.8V, C _L =50pF | — | 40 | |
| | Output high/ low to low/ high level fall/ rise time | V _{DD} =1.8V, C _L =10pF | — | 3.6/3.2 | ns |
| | | V _{DD} =1.8V, C _L =30pF | 8.0/5.0 | 7.4/4.0 | |
| | | V _{DD} =1.8V, C _L =50pF | — | 7.8/6.2 | |
| GPIOx_OSPD0->OSPDy[1:0] =X0 (IO_Speed = 2MHz) | Maximum frequency ⁽³⁾ | V _{DD} =3.3V, C _L =10pF | 2 | 16 | MHz |
| | | V _{DD} =3.3V, C _L =30pF | 2 | 16 | |
| | | V _{DD} =3.3V, C _L =50pF | 2 | 12 | |
| | Output high/ low to low/ high level fall/ rise time | V _{DD} =3.3V, C _L =10pF | 13.8/11.4 | 16.4/11.8 | ns |
| | | V _{DD} =3.3V, C _L =30pF | 19.0/14.8 | 19.2/17.8 | |
| | | V _{DD} =3.3V, C _L =50pF | 28.2/22.8 | 27.2/24.4 | |
| GPIOx_OSPD0->OSPDy[1:0] =01 | Maximum frequency ⁽³⁾ | V _{DD} =3.3V, C _L =10pF | 10 | 72 | MHz |
| | | V _{DD} =3.3V, C _L =30pF | 10 | 72 | |

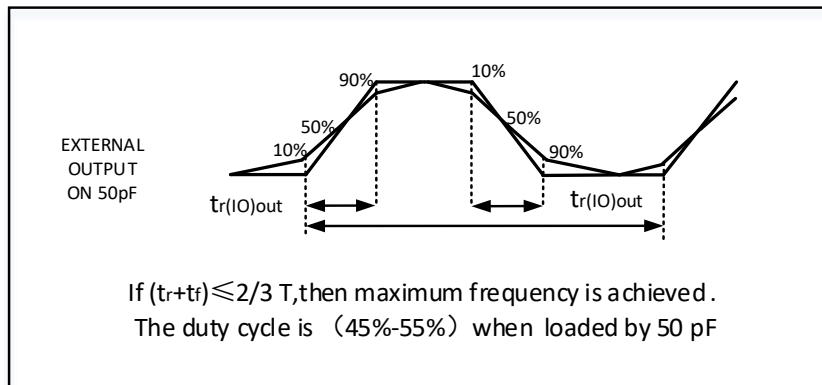
| GPIOx_OSPD[1:0] bit value | Parameter | Conditions | Typ | Max | Unit |
|--|---|---|-----------|-----------|------|
| (IO_Speed = 10MHz) | | V _{DD} =3.3V, C _L =50pF | 10 | 40 | |
| | Output high/ low to low/ high level fall/ rise time | V _{DD} =3.3V, C _L =10pF | 3.4/2.8 | 4.0/3.4 | ns |
| | | V _{DD} =3.3V, C _L =30pF | 4.6/3.4 | 5.2/4.0 | |
| | | V _{DD} =3.3V, C _L =50pF | 8.0/6.4 | 8.2/6.2 | |
| GPIOx_OSPD0->OSPDy[1:0] =11 (IO_Speed = 50MHz) | Maximum frequency ⁽³⁾ | V _{DD} =3.3V, C _L =10pF | — | 32 | MHz |
| | | V _{DD} =3.3V, C _L =30pF | — | 46 | |
| | | V _{DD} =3.3V, C _L =50pF | — | 40 | |
| | Output high/ low to low/ high level fall/ rise time | V _{DD} =3.3V, C _L =10pF | — | 2.4/2.6 | ns |
| | | V _{DD} =3.3V, C _L =30pF | — | 2.6/2.4 | |
| | | V _{DD} =3.3V, C _L =50pF | — | 8.4/3.2 | |
| GPIOx_OSPD0->OSPDy[1:0] =X0 (IO_Speed = 2MHz) | Maximum frequency ⁽³⁾ | V _{DD} =3.6V, C _L =10pF | 2 | 16 | MHz |
| | | V _{DD} =3.6V, C _L =30pF | 2 | 16 | |
| | | V _{DD} =3.6V, C _L =50pF | 2 | 12 | |
| | Output high/ low to low/ high level fall/ rise time | V _{DD} =3.6V, C _L =10pF | 13.2/10.6 | 12.0/10.4 | ns |
| | | V _{DD} =3.6V, C _L =30pF | 17.2/14.4 | 18.8/15.4 | |
| | | V _{DD} =3.6V, C _L =50pF | 26.8/22.2 | 26.4/21.8 | |
| GPIOx_OSPD0->OSPDy[1:0] =01 (IO_Speed = 10MHz) | Maximum frequency ⁽³⁾ | V _{DD} =3.6V, C _L =10pF | 10 | 72 | MHz |
| | | V _{DD} =3.6V, C _L =30pF | 10 | 72 | |
| | | V _{DD} =3.6V, C _L =50pF | 10 | 40 | |
| | Output high/ low to low/ high level fall/ rise time | V _{DD} =3.6V, C _L =10pF | 3.2/2.8 | 3.6/3.2 | ns |
| | | V _{DD} =3.6V, C _L =30pF | 3.8/3.2 | 4.4/3.4 | |
| | | V _{DD} =3.6V, C _L =50pF | 7.6/6.0 | 8.0/6.0 | |
| GPIOx_OSPD0->OSPDy[1:0] =11 (IO_Speed = 50MHz) | Maximum frequency ⁽³⁾ | V _{DD} =3.6V, C _L =10pF | — | 42 | MHz |
| | | V _{DD} =3.6V, C _L =30pF | — | 46 | |
| | | V _{DD} =3.6V, C _L =50pF | — | 36 | |
| | Output high/ low to low/ high level fall/ rise time | V _{DD} =3.6V, C _L =10pF | — | 3.0/9.6 | ns |
| | | V _{DD} =3.6V, C _L =30pF | — | 2.4/2.4 | |
| | | V _{DD} =3.6V, C _L =50pF | — | 3.2/3.2 | |

(1) Based on characterization, not actual test values.

(2) The I/O speed is configured using the GPIOx_OSPD0->OSPDy [1:0] bits. Refer to the GD32E230xx user manual which is selected to set the GPIO port output speed.

(3) The maximum frequency is defined in [Figure 4-1. I/O port AC characteristics definition](#)

Figure 4-1. I/O port AC characteristics definition



4.13 ADC characteristics

Table 4-19. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------------|--|---------------------------------|-------|------------------|-------------------|------------------------|
| V _{DDA} | Operating voltage | — | 2.4 | 3.3 | 3.6 | V |
| V _{IN} | ADC input voltage range | — | 0 | — | V _{REF+} | V |
| f _{ADC} | ADC clock | — | 0.1 | — | 28 | MHZ |
| f _s ⁽¹⁾ | Sampling rate | 12-bit | 0.007 | — | 2 | MSP S |
| | | 10-bit | 0.008 | — | 2.3 | |
| | | 8-bit | 0.01 | — | 2.8 | |
| | | 6-bit | 0.011 | — | 3.5 | |
| V _{IN} | Analog input voltage | 10 external;2 internal | 0 | — | V _{DDA} | V |
| V _{REF+} | Positive Reference Voltage | — | — | V _{DDA} | — | V |
| V _{REF-} | Negative Reference Voltage | — | — | 0 | — | V |
| R _{AIN} ⁽¹⁾ | External input impedance | See Equation 2 | — | — | 50.6 | kΩ |
| R _{ADC} ⁽¹⁾ | Input sampling switch resistance | — | — | — | 0.5 | kΩ |
| C _{ADC} ⁽¹⁾ | Input sampling capacitance | No pin/pad capacitance included | — | — | 4 | pF |
| t _{CAL} | Calibration time | f _{ADC} =28MHZ | — | 4.68 | — | μs |
| t _s | Sampling time | f _{ADC} =28MHZ | 0.05 | — | 8.55 | μs |
| t _{CONV} ⁽¹⁾ | Total conversion time(including sampling time) | 12-bit | — | 14 | — | 1/ f _{ADC} |
| | | 10-bit | — | 12 | — | |
| | | 8-bit | — | 10 | — | |
| | | 6-bit | — | 8 | — | |
| t _{SU} ⁽¹⁾ | Startup time | — | — | — | 1 | μs |

(1).Based on design, not actual test values.

Equation 2: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N=12 (from 12-bit resolution).

Table 4-20. ADC R_{AIN} max for f_{ADC} = 28MHz⁽¹⁾

| T _s (cycles) | t _s (us) | R _{AIN} max (KΩ) |
|-------------------------|---------------------|---------------------------|
| 1.5 | 0.05 | 0.88 |
| 7.5 | 0.27 | 6.4 |
| 13.5 | 0.48 | 11.9 |
| 28.5 | 1.02 | 25.7 |
| 41.5 | 1.48 | 37.7 |
| 55.5 | 1.98 | 50.6 |
| 71.5 | 2.55 | NA |
| 239.5 | 8.55 | NA |

(1). Based on design, not actual test values.

4.14 Temperature sensor characteristics

Table 4-261. Temperature sensor characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|--|--|-----|------|-----|-------|
| T _L ⁽¹⁾ | V _{SENSE} linearity with temperature | — | ±1.5 | — | °C |
| Avg_Slope ⁽¹⁾ | Average slope | — | 4.3 | — | mV/°C |
| V ₂₅ ⁽¹⁾ | Voltage at 25 °C | — | 1.45 | — | V |
| t _{START} ⁽²⁾ | Startup time | — | — | — | μs |
| t _{s_temp} ^{(2) (3)} | ADC sampling time when reading the temperature | — | 17.1 | — | μs |

(1). Based on characterization, not actual test values.

(2). Based on design, not actual test values.

(3). Shortest sampling time can be determined in the application.

4.15 Comparators characteristics

Table 4-272. CMP characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max ⁽¹⁾ | Unit |
|------------------|---|-----------------------|-----|------|--------------------|------|
| V _{DDA} | Operating voltage | — | 1.8 | 3.3 | 3.6 | V |
| V _{IN} | Input voltage range | — | 0 | — | V _{DDA} | V |
| V _{BG} | Scaler input voltage | — | — | 1.2 | — | V |
| V _{SC} | Scaler offset voltage | — | — | — | — | mV |
| t _D | Propagation delay for 200mv step with 100mV overdrive | Ultra low power mode | — | 0.98 | — | μs |
| | | Low power mode | — | 0.25 | — | μs |
| | | Medium power mode | — | 0.12 | — | μs |
| | | High speed power mode | — | 33 | — | μs |
| | Propagation delay for full range step with 100mV | Ultra low power mode | — | — | — | μs |
| | | Low power mode | — | — | — | μs |

| Symbol | Parameter | Conditions | Min | Typ | Max ⁽¹⁾ | Unit |
|---------------------|---------------------|-----------------------|-----|------|--------------------|------|
| | overdrive | Medium power mode | — | — | — | μs |
| | | High speed power mode | — | — | — | ns |
| I _{DD} | Current consumption | Ultra low power mode | — | 2.2 | — | μA |
| | | Low power mode | — | 3.2 | — | |
| | | Medium power mode | — | 8.1 | — | |
| | | High speed power mode | — | 46.9 | — | |
| V _{offset} | Offset error | — | — | ±4 | — | mV |
| V _{hyst} | Hysteresis Voltage | No Hysteresis | — | 0 | — | mV |
| | | Low Hysteresis | — | 11 | — | |
| | | Medium Hysteresis | — | 22 | — | |
| | | High Hysteresis | — | 43 | — | |

(1). Based on characterization, not actual test values.

4.16 TIMER characteristics

Table 4-283. TIMER characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------------|---|---------------------------------|--------|---------------------------|------------------------|
| t _{res} | Timer resolution time | — | 1 | — | t _{TIMERxCLK} |
| | | f _{TIMERxCLK} = 72 MHz | 13.9 | — | ns |
| f _{EXT} | Timer external clock frequency | — | 0 | f _{TIMERxCLK} /2 | MHz |
| | | f _{TIMERxCLK} = 72 MHz | 0 | 36 | MHz |
| RES | Timer resolution | — | — | 16 | bit |
| t _{COUNTER} | 16-bit counter clock period when internal clock is selected | — | 1 | 65536 | t _{TIMERxCLK} |
| | | f _{TIMERxCLK} = 72 MHz | 0.0139 | 910 | μs |
| t _{MAX_COUNT} | Maximum possible count | — | — | 65536 × 65536 | t _{TIMERxCLK} |
| | | f _{TIMERxCLK} = 72 MHz | — | 59.6 | s |

4.17 WDGT characteristics

Table 4-29. FWDGT min/max timeout period at 40 kHz (IRC40K)

| Prescaler divider | PR[2:0] bits | Min timeout RLD[11:0]= 0x000 | Max timeout RLD[11:0]= 0xFFFF | Unit |
|-------------------|--------------|---------------------------------|----------------------------------|------|
| 1/4 | 000 | 0.1 | 409.6 | ms |
| 1/8 | 001 | 0.2 | 819.2 | |
| 1/16 | 010 | 0.4 | 1638.4 | |
| 1/32 | 011 | 0.8 | 3276.8 | |
| 1/64 | 100 | 1.6 | 6553.6 | |
| 1/128 | 101 | 3.2 | 13107.2 | |
| 1/256 | 110 or 111 | 6.4 | 26214.4 | |

Table 4-305. WWDGT min-max timeout value @72 MHz (f_{PCLK1})

| Prescaler divider | PSC[2:0] | Min timeout value CNT[6:0] = 0x40 | Unit | Max timeout value CNT[6:0] = 0x7F | Unit |
|-------------------|----------|--------------------------------------|------|--------------------------------------|------|
| 1/1 | 00 | 56.9 | μs | 3.64 | ms |
| 1/2 | 01 | 113.8 | | 7.28 | |
| 1/4 | 10 | 227.6 | | 14.56 | |
| 1/8 | 11 | 455.1 | | 29.13 | |

4.18 I2C characteristics

Table 4-316. I2C characteristics

| Symbol | Parameter | Condi tions | Standard mode ⁽¹⁾ | | Fast mode ^{(1) (2)} | | Unit |
|------------------|---------------------------|----------------|------------------------------|------|------------------------------|------|------|
| | | | Min | Max | Min | Max | |
| f_{SCL} | SCL clock frequency | — | 0 | 100 | 0 | 1000 | KHz |
| $t_{SCL(H)}$ | SCL clock high time | — | 4.0 | — | 0.6 | — | μs |
| $t_{SCL(L)}$ | SCL clock low time | — | 4.7 | — | 1.3 | — | μs |
| $t_{su(SDA)}$ | SDA setup time | — | 250 | — | 100 | — | ns |
| $t_{h(SDA)}$ | SDA data hold time | — | 0 ⁽³⁾ | 3450 | 0 | 900 | ns |
| $t_{r(SDA/SCL)}$ | SDA and SCL rise time | — | — | 1000 | — | 300 | ns |
| $t_{f(SDA/SCL)}$ | SDA and SCL fall time | — | — | 300 | — | 300 | ns |
| $t_{h(STA)}$ | Start condition hold time | — | 4.0 | — | 0.6 | — | us |

(1) Based on design, not actual test values.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode puls I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

4.19 SPI characteristics

Table 4-327. Standard SPI characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|------------------------|------------|-----|-----|-----|------|
| f_{SCK} | SCK clock frequency | — | — | — | 18 | MHz |
| $t_{sck(H)}$ | SCK clock high time | — | 25 | 27 | 29 | ns |
| $t_{sck(L)}$ | SCK clock low time | — | 25 | 27 | 29 | ns |
| SPI master mode | | | | | | |
| $t_{v(MO)}$ | Data output valid time | — | — | — | 2 | ns |
| $t_{su(MI)}$ | Data input setup time | — | 5 | — | — | ns |
| $t_{h(MI)}$ | Data input hold time | — | 5 | — | — | ns |
| SPI slave mode | | | | | | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|--------------------------|------------------|-------------|-----|-----|------|
| $t_{SU(NSS)}$ | NSS enable setup time | $f_{PCLK}=72MHz$ | $4T_{PCLK}$ | — | — | ns |
| $t_{H(NSS)}$ | NSS enable hold time | $f_{PCLK}=72MHz$ | $2T_{PCLK}$ | — | — | ns |
| $t_{A(SO)}$ | Data output access time | $f_{PCLK}=72MHz$ | 2 | — | 55 | ns |
| $t_{DIS(SO)}$ | Data output disable time | — | 3 | — | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | — | — | — | 29 | ns |
| $t_{SU(SI)}$ | Data input setup time | — | 2 | — | — | ns |
| $t_{H(SI)}$ | Data input hold time | — | 0 | — | — | ns |

(1). Data based on characterization results, not tested in production.

4.20 I2S characteristics

Table 4-338. I2S characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|----------------------------------|--|-----|-----|-------|------|
| f_{CK} | Clock frequency | Master mode (data: 16 bits, Audio frequency = 48 kHz) | — | — | 6 | MHz |
| | | Slave mode | — | — | 6 | |
| t_H | Clock high time | $f_{CK}=6MHz$ | — | — | 83.33 | ns |
| t_L | Clock low time | | — | — | 83.33 | ns |
| $t_{V(WS)}$ | WS valid time | Master mode | 0 | — | 2 | ns |
| $t_{H(WS)}$ | WS hold time | Master mode | 0 | — | — | ns |
| $t_{SU(WS)}$ | WS setup time | Slave mode | 0 | — | — | ns |
| $t_{H(WS)}$ | WS hold time | Slave mode | 0.5 | — | — | ns |
| $DuCy(SCK)$ | I2S slave input clock duty cycle | Slave mode | 30 | — | 70 | % |
| $t_{SU(SD_MR)}$ | Data input setup time | Master mode | 2 | — | — | ns |
| $t_{SU(SD_SR)}$ | Data input setup time | Slave mode | 0 | — | — | ns |
| $t_{H(SD_MR)}$ | Data input hold time | Master receiver | 1.5 | — | — | ns |
| $t_{H(SD_SR)}$ | | Slave receiver | 1.5 | — | — | ns |
| $t_{V(SD_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | — | — | 11 | ns |
| $t_{H(SD_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 3 | — | — | ns |
| $t_{V(SD_MT)}$ | Data output valid time | Master transmitter (after enable edge) | — | — | 11 | ns |
| $t_{H(SD_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 0 | — | — | ns |

(1). Data based on characterization results, not tested in production.

4.21 USART characteristics

Table 4-349. USART characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---------------------|------------|------|-----|-----|------|
| f _{SCK} | SCK clock frequency | — | — | — | 36 | MHz |
| TSI _{K(H)} | SCK clock high time | — | 13.5 | — | — | ns |
| TSI _{K(L)} | SCK clock low time | — | 13.5 | — | — | ns |

(1). Data based on characterization results, not tested in production.

5 Package information

5.1 TSSOP package outline dimensions

Figure 5-1. TSSOP package outline

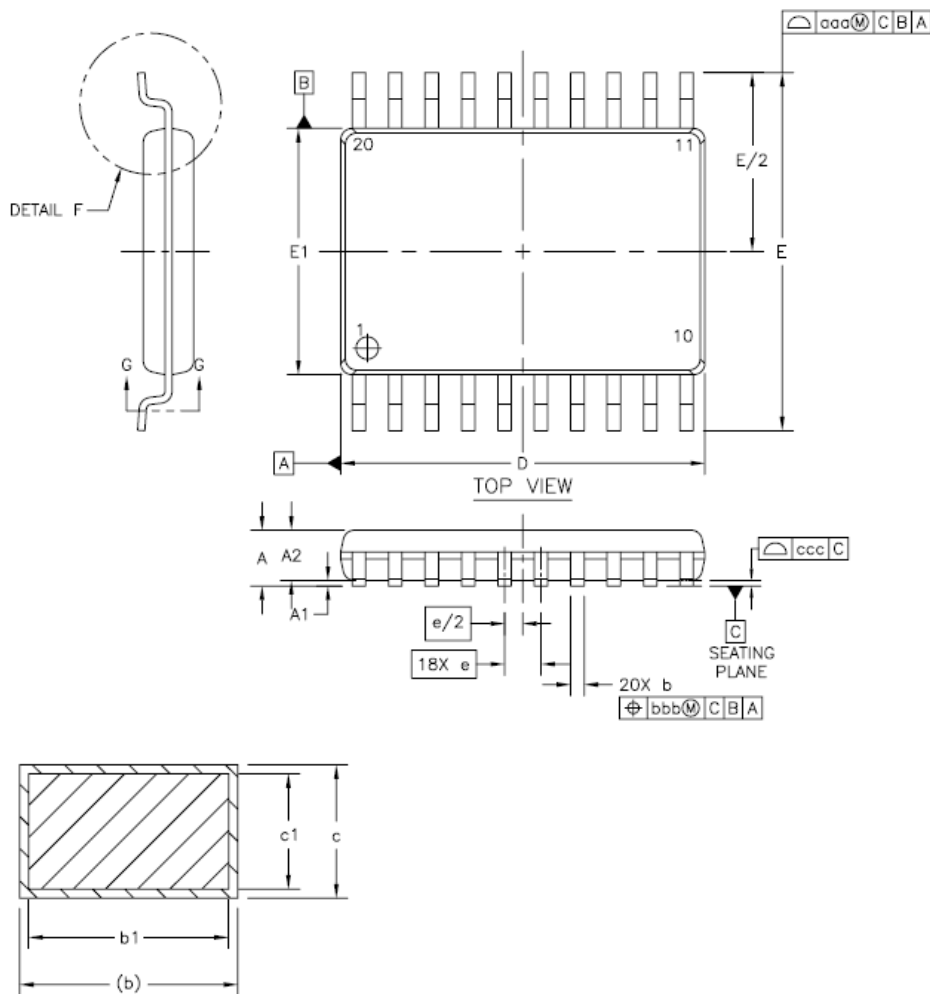


Table 5-1. TSSOP20 package dimensions

| Symbol | Dimensions (mm) | | | Symbol | Dimensions (mm) | | |
|--------|-----------------|------|------|--------|-----------------|-----|------|
| | Min | Typ | Max | | Min | Typ | Max |
| A | - | - | 1.2 | c1 | 0.09 | - | 0.16 |
| A1 | 0.05 | - | 1.15 | D | 6.4 | 6.5 | 6.6 |
| A2 | 0.80 | 1.00 | 1.05 | E1 | 4.3 | 4.4 | 4.5 |
| b | 0.19 | - | 0.30 | E | 6.40 | | |
| B1 | 0.19 | 0.22 | 0.25 | e | 0.65 | | |
| c | 0.09 | - | 0.20 | L | 0.45 | 0.6 | 0.75 |

5.2 LGA package outline dimensions

Figure 5-2. LGA20 package outline

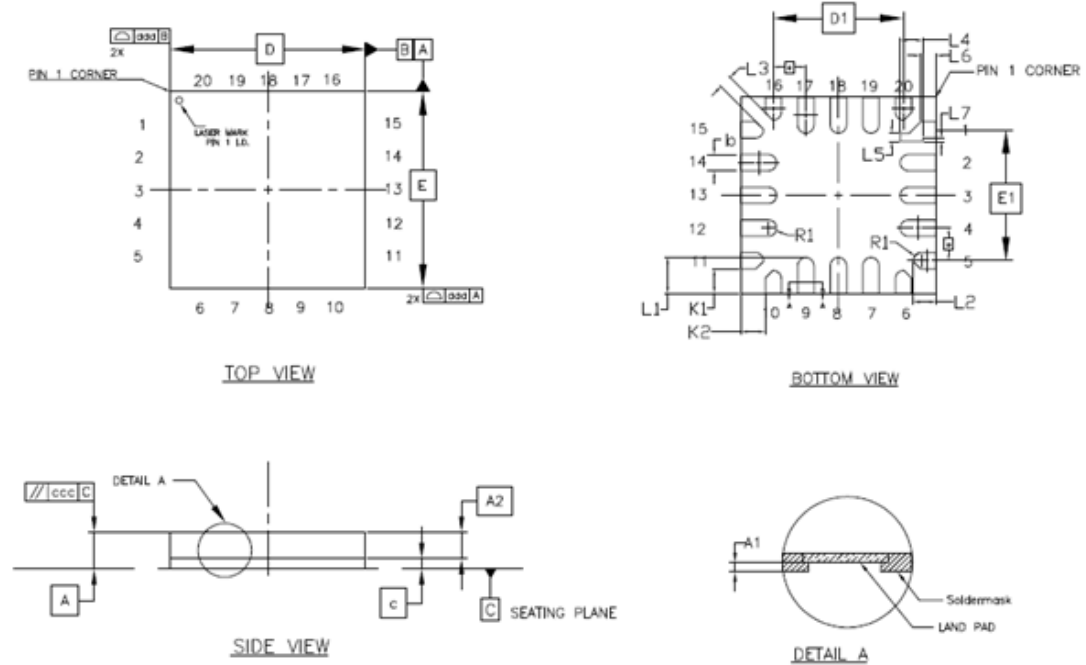


Table 5-2. LGA20 package dimensions

| Symbol | LGA20 | | |
|--------|------------|-------|-------|
| | Min | Typ | Max |
| A | 0.51 | 0.56 | 0.61 |
| A1 | - | 0.015 | 0.022 |
| A2 | 0.35 | 0.40 | 0.45 |
| c | 0.13 | 0.16 | 0.19 |
| D | 2.90 | 3.00 | 3.10 |
| D1 | 1.95 | 2.00 | 2.05 |
| E | 2.90 | 3.00 | 3.10 |
| E1 | 1.95 | 2.00 | 2.05 |
| e | 0.50 BASIC | | |
| L1 | 0.50 | 0.55 | 0.60 |
| L2 | 0.30 | 0.35 | 0.40 |
| L3 | 0.200 REF | | |
| L4 | 0.30 | 0.35 | 0.40 |
| L5 | 0.125 REF | | |
| L6 | 0.234 REF | | |
| L7 | 0.050 REF | | |
| R1 | 0.125 REF | | |
| K1 | 0.375 REF | | |
| K2 | 0.375 REF | | |

| Symbol | LGA20 | | |
|--------|-------|------|------|
| | Min | Typ | Max |
| b | 0.20 | 0.25 | 0.30 |
| aaa | 0.100 | | |
| ccc | 0.100 | | |

(Original dimensions are in millimeters)

5.3 QFN package outline dimensions

Figure 5-3. QFN package outline

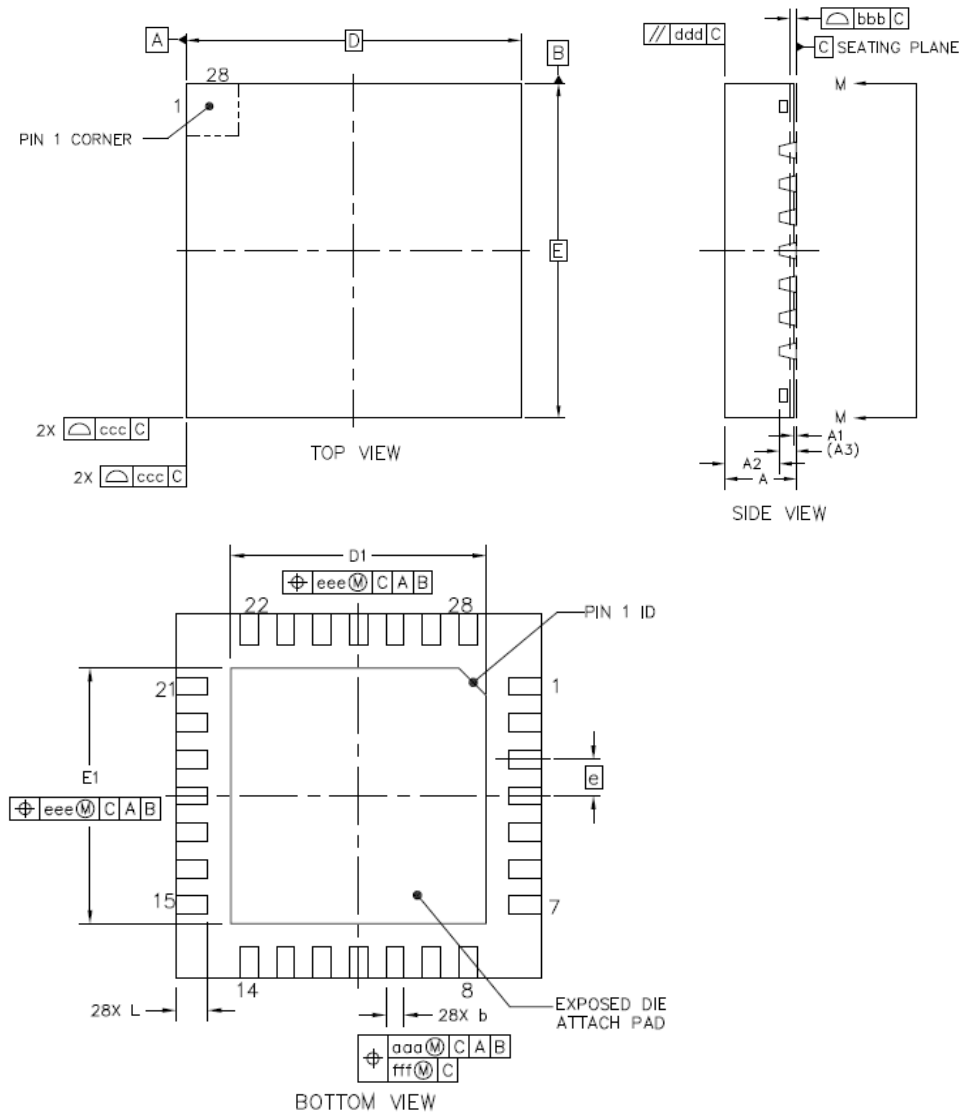


Table 5-3. QFN package dimensions

| Symbol | QFN28 | | | QFN32 | | |
|--------|-------|-------|------|-------|-------|------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.8 | 0.85 | 0.9 | 0.8 | 0.85 | 0.9 |
| A1 | 0 | 0.035 | 0.05 | 0 | 0.035 | 0.05 |
| A2 | - | 0.65 | 0.67 | - | 0.65 | 0.67 |
| A3 | - | 0.203 | - | - | 0.203 | - |
| D | - | 4.0 | - | - | 5.0 | - |
| E | - | 4.0 | - | - | 5.0 | - |
| D1 | 2.7 | 2.8 | 2.9 | 3.4 | 3.5 | 3.6 |
| E1 | 2.7 | 2.8 | 2.9 | 3.4 | 3.5 | 3.6 |
| L | 0.25 | 0.35 | 0.45 | 0.3 | 0.4 | 0.5 |
| e | 0.4 | | | 0.5 | | |
| b | 0.15 | 0.2 | 0.25 | 0.2 | 0.25 | 0.3 |

(Original dimensions are in millimeters)

5.4 LQFP package outline dimensions

Figure 5-4. LQFP package outline

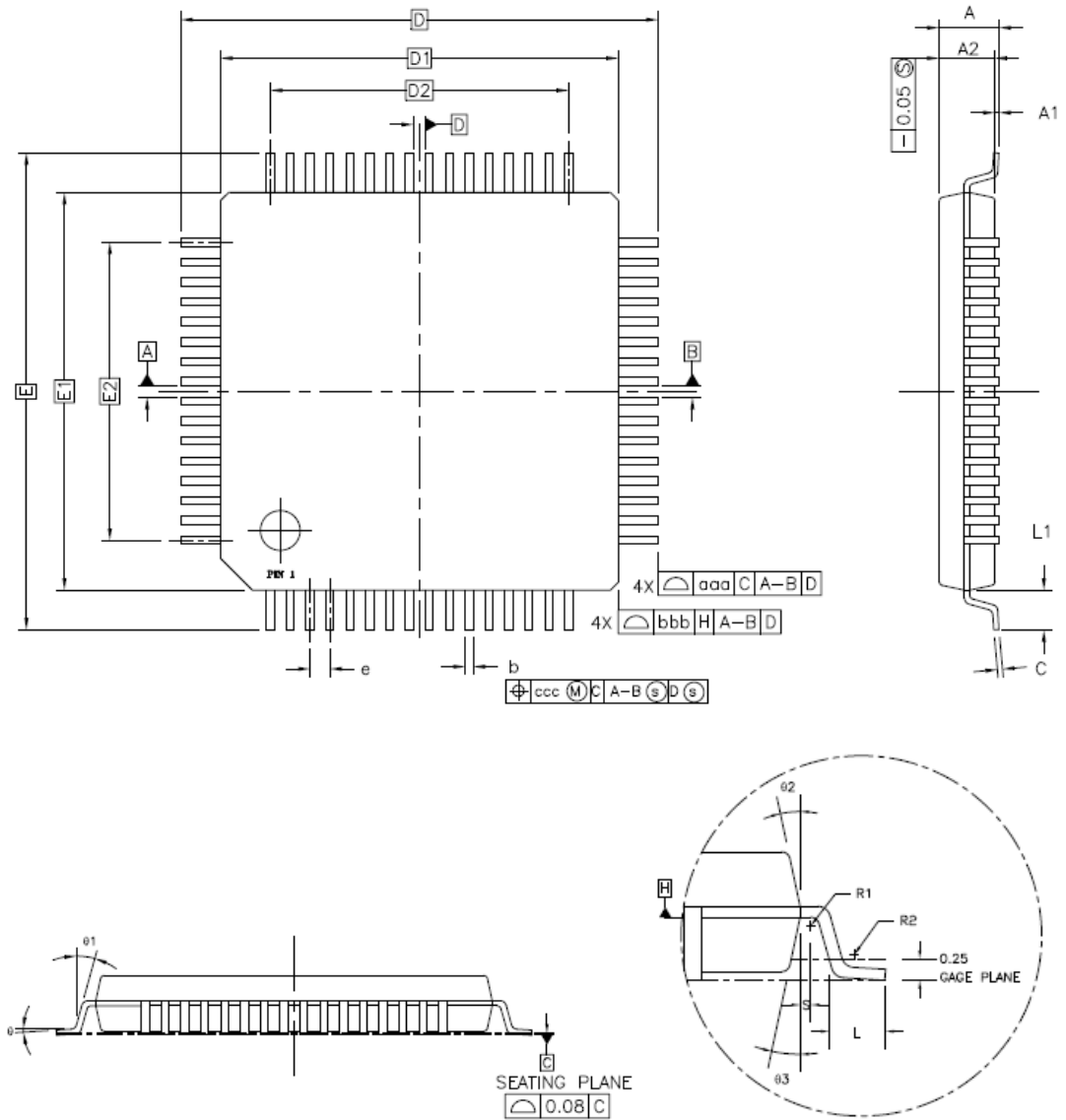


Table 5-4. LQFP package dimensions

| Symbol | LQFP32 | | | LQFP48 | | |
|------------|--------|------|------|--------|------|------|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.60 | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 | 1.35 | 1.40 | 1.45 |
| D | - | 9.00 | - | - | 9.00 | - |
| D1 | - | 7.00 | - | - | 7.00 | - |
| E | - | 9.00 | - | - | 9.00 | - |
| E1 | - | 7.00 | - | - | 7.00 | - |
| R1 | 0.08 | - | - | 0.08 | - | - |
| R2 | 0.08 | - | 0.20 | 0.08 | - | 0.20 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ_1 | 0° | - | - | 0° | - | - |
| θ_2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ_3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | - | 0.20 | 0.09 | - | 0.20 |
| L | 0.45 | 0.60 | 0.75 | 0.45 | 0.60 | 0.75 |
| L1 | - | 1.00 | - | - | 1.00 | - |
| S | 0.20 | - | - | 0.20 | - | - |
| b | 0.33 | - | 0.41 | 0.17 | 0.22 | 0.27 |
| e | - | 0.80 | - | - | 0.50 | - |
| D2 | - | 5.50 | - | - | 5.50 | - |
| E2 | - | 5.50 | - | - | 5.50 | - |
| aaa | 0.20 | | | 0.20 | | |
| bbb | 0.20 | | | 0.20 | | |
| ccc | 0.08 | | | 0.08 | | |

(Original dimensions are in millimeters)

6 Ordering information

Table 6-1. Part ordering code for GD32E230xx devices

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---------------|------------|---------|--------------|------------------------------|
| GD32E230F4V6 | 16 | LGA20 | Green | Industrial -40°C to +85°C |
| GD32E230F6V6 | 32 | LGA20 | Green | Industrial -40°C to +85°C |
| GD32E230F8V6 | 64 | LGA20 | Green | Industrial -40°C to +85°C |
| GD32E230F4P6 | 16 | TSSOP20 | Green | Industrial -40°C to +85°C |
| GD32E230F6P6 | 32 | TSSOP20 | Green | Industrial -40°C to +85°C |
| GD32E230F8P6 | 64 | TSSOP20 | Green | Industrial -40°C to +85°C |
| GD32E230G4U6 | 16 | QFN28 | Green | Industrial -40°C to +85°C |
| GD32E230G6U6 | 32 | QFN28 | Green | Industrial -40°C to +85°C |
| GD32E230G8U6 | 64 | QFN28 | Green | Industrial -40°C to +85°C |
| GD32E230K4U6 | 16 | QFN32 | Green | Industrial -40°C to +85°C |
| GD32E230K6U6 | 32 | QFN32 | Green | Industrial -40°C to +85°C |
| GD32E230K8U6 | 64 | QFN32 | Green | Industrial -40°C to +85°C |
| GD32E230K4T6 | 16 | LQFP32 | Green | Industrial -40°C to +85°C |
| GD32E230K6T6 | 32 | LQFP32 | Green | Industrial -40°C to +85°C |
| GD32E230K8T6 | 64 | LQFP32 | Green | Industrial -40°C to +85°C |
| GD32E230C4T6 | 16 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32E230C6T6 | 32 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32E230C8T6 | 64 | LQFP48 | Green | Industrial -40°C to +85°C |

7 Revision history

Table 7-1. Revision history

| Revision No. | Description | Date |
|--------------|---|-------------|
| 1.0 | Initial Release | Oct10, 2018 |
| 1.1 | Add information about the QFN20 package | Dec7, 2018 |
| 1.2 | Delete QFN20 package, add information about the LGA20 package and electrical characteristics with few changes | Dec28, 2018 |

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