Texas Instruments

TCAN1042-Q1, TCAN1042V-Q1, TCAN1042H-Q1
TCAN1042HV-Q1, TCAN1042G-Q1, TCAN1042GV-Q1
TCAN1042HG-Q1, TCAN1042HGV-Q1

SLLSES9 – FEBRUARY 2016

TCAN1042-Q1 Automotive Fault Protected CAN Tranceiver with CAN FD

1 Features

- Qualified for Automotive Applications
- Meets the Requirements of ISO11898-2 (2016)
- 'Turbo' CAN:
  - All devices support 2 Mbps CAN FD (Flexible Data Rate) and "G" options support 5 Mbps
  - Short and Symmetrical Propagation Delay Times and Fast Loop Times for Enhanced Timing Margin
  - Higher Data Rates in Loaded CAN Networks
- I/O Voltage Range Supports 3.3 V and 5 V MCUs
- Ideal Passive Behavior When Unpowered
  - Bus and Logic Terminals are High Impedance (no load)
  - Power Up/Down With Glitch Free Operation On Bus and RXD Output
- Protection Features
  - HBM ESD Protection Exceeds ±10 kV
  - IEC ESD Protection Exceeds ±8 kV
  - Bus Fault Protection: ±58 V and ±70 V Variants
  - Undervoltage Protection on V_{CC} and V_{IO} Supply Terminals
  - Driver Dominant Time Out (TXD DTO) - Data rates down to 10kbps
  - Thermal Shutdown Protection
- Characterized for Ambient Temeratures from –55°C to 125°C

2 Applications

- All devices support "Classical CAN" and CAN FD applications up to 2 Mbps
- "G" devices support CAN FD applications up to 5 Mbps Operation
- All devices support highly loaded CAN networks
- Automotive and Transportation

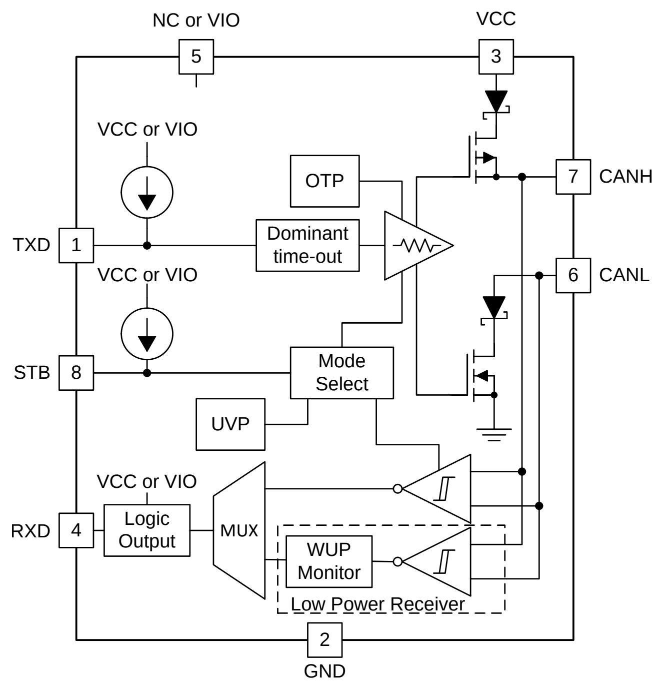
3 Description

This CAN transceiver family meets the ISO11898-2 (2016) High Speed CAN (Controller Area Network) physical layer standard. All devices are designed for use in CAN FD networks up to 2 Mbps (megabits per second). Devices with part numbers that include the "G" suffix are designed for data rates up to 5 Mbps, and versions with the "V" have a secondary power supply input for I/O level shifting the input pin thresholds and RXD output level. This family has a low power standby mode with remote wake request feature. Additionally, all devices include many protection features to enhance device and CAN-network robustness.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TCAN1042x-Q1	SOIC (8)	4.90 mm × 3.91 mm

Functional Block Diagram



A. Terminal 5 function is device dependent; NC on devices without the "V" suffix, and V_{IO} for I/O level shifting for devices with the "V" suffix.

B. RXD logic output is driven to V_{CC} on devices without the "V" suffix, and V_{IO} for devices with the "V" suffix.

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4 Revision History

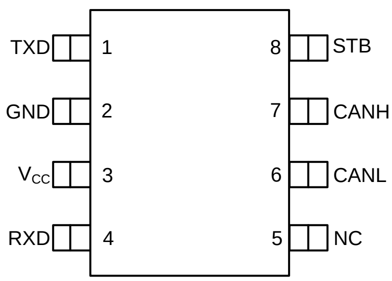
DATE	REVISION	NOTES
February 2016	*	Initial release.

5 Device Comparison Table

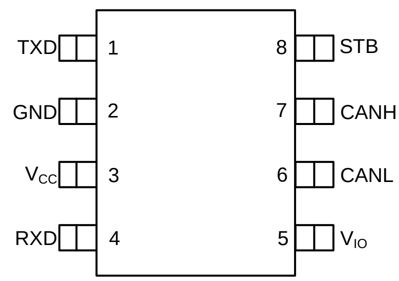
DEVICE NUMBER	BUS FAULT PROTECTION	5-Mbps FLEXIBLE DATA RATE	3-V LEVEL SHIFTER INTEGRATED	PIN 8 MODE SELECTION
TCAN1042-Q1 (Base)	**±58 V**			Low Power Standby Mode with Remote Wake
TCAN1042G-Q1	**±58 V**	**X**		
TCAN1042GV-Q1	**±58 V**	**X**	**X**	
TCAN1042V-Q1	**±58 V**		**X**	
TCAN1042H-Q1	**±70 V**			
TCAN1042HG-Q1	**±70 V**	**X**		
TCAN1042HGV-Q1	**±70 V**	**X**	**X**	
TCAN1042HV-Q1	**±70 V**		**X**	

6 Pin Configurations and Functions

D Package for Base, (H), (G), and (HG)
8 PIN (SOIC)
Top View



D Package for (V), (HV), (GV), and (HGV)
8 PIN (SOIC)
Top View



Pin Functions

PINS			TYPE	DESCRIPTION
NAME	Base, (H), (G), (HG)	(V), (HV), (GV), (HGV)		
TXD	1	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND	2	2	GND	Ground connection
VCC	3	3	I	Transceiver 5-V supply voltage
RXD	4	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
NC	5	—	—	No Connect
V_{IO}	—	5	I	Transceiver I/O level shifting supply voltage (Devices with "V" suffix only)
CANL	6	6	I/O	Low level CAN bus line
CANH	7	7	I/O	High level CAN bus line
STB	8	8	I	Standby Mode control input (active high)

7 Specifications

7.1 Absolute Maximum Ratings(1) (2)

			MIN	MAX	UNIT
V_{CC}	5V bus supply voltage range		–0.3	+7	V
V_{IO}	I/O Level Shifting Voltage Range	Devices with the "V" suffix	–0.3	+7	
V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)	Devices without the "H" suffix	-58	+58	
V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)	Devices with the "H" suffix	-70	+70	
$V_{(Logic\_Input)}$	Logic input terminal voltage range (TXD, STB)		–0.3	+7 and $V_I \le V_{IO}$ + 0.3	
$V_{(Logic\_Output)}$	Logic output terminal voltage range (RXD)		–0.3	+7 and $V_I \le V_{IO}$ + 0.3	
$I_{O(RXD)}$	RXD (Receiver) output current		-8	+8	mA
T_J	Operating virtual junction temperature range (see Thermal Information)		–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

7.2 ESD Ratings

	TEST CONDITIONS		VALUE	UNIT
Human Body Model (HBM) ESD stress voltage	All terminals(1)		±6000	V
	CAN bus terminals (CANH, CANL) to GND(2)		±10000	
Charged Device Model (CDM) ESD stress voltage	All terminals(3)		±750	V
Machine Model (MM)	All terminals(4)		±200	
System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10605: Powered Air Discharge	±15000	V
		SAE J2962-2 per ISO 10605: Powered Contact Discharge	±8000	
System Level Electro-Static Discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	IEC 61400-4-2: Unpowered Air Discharge	±15000	V
		IEC 61400-4-2: Powered on Contact Discharge	±8000	
ISO7637-2 Transients according to GIFT - ICT CAN EMC test specification(5)	CAN bus terminals (CANH, CANL) to GND	Pulse 1	–100	V
		Pulse 2	+75	
		Pulse 3a	–150	
		Pulse 3b	+100	
ISO7637-3 Transients	CAN bus terminals (CANH, CANL) to GND	Direct Coupling Capacitor "Slow Transient Pulse" with 100nF coupling capacitor - Powered	±85	

(1) Tested in accordance to JEDEC Standard 22, Test Method A114.
(2) Test method based upon JEDEC Standard 22 Test Method A114, CAN bus is stressed with respect to GND.
(3) Tested in accordance to JEDEC Standard 22, Test Method C101.
(4) Tested in accordance to JEDEC Standard 22, Test Method A115.
(5) ISO7637 is a system level transient test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. Different system level configurations may lead to different results.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	5V Bus Supply Voltage Range	4.5	5.5	V
V_{IO}	I/O Level Shifting Voltage Range	3	5.5	
$I_{OH(RXD)}$	RXD terminal HIGH level output current	–2		mA
$I_{OL(RXD)}$	RXD terminal LOW level output current		2	

7.4 Thermal Information

THERMAL METRIC(1)		TEST CONDITIONS	TCAN1042-Q1 D (SOIC) 8 Pins	UNIT
$R_{\theta JA}$	Junction-to-air thermal resistance	High-K thermal resistance(2)	105.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(3)		46.8	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance(4)		48.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter(5)		8.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter(6)		46.2	°C/W
P_D	Average power dissipation	V_{CC} = 5 V, V_{RXD} = 5 V, T_J = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 250 kHz, 25% duty cycle square wave, C_{L_RXD} = 15 pF. Typical CAN operating conditions at 500kbps with 25% transmission (dominant) rate.	115	mW
		V_{CC} = 5.5 V, V_{RXD} = 5.5 V, T_J = 150°C, R_L = 50 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_{L_RXD} = 15 pF. Typical high load CAN operating conditions at 1 Mbps with 50% transmission (dominant) rate and loaded network.	268	
	Thermal shutdown temperature		170	°C
	Thermal shutdown hysteresis		5	°C

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, Ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

7.5 Electrical Characteristics

Over recommended operating conditions with T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
SUPPLY CHARACTERISTICS							
I_{CC}	5-V Supply current	Normal Mode (Driving Dominant)	See Figure 5, TXD = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open, STB = 0 V, Typical Bus Load		40	70	mA
		Normal Mode (Driving Dominant)	See Figure 5, TXD = 0 V, R_L = 50 Ω, C_L = open, R_{CM} = open, STB = 0 V, High Bus Load		45	80	mA
		Normal Mode (Driving Dominant – with bus fault)	See Figure 5, TXD = 0 V, STB = 0V, CANH = -12V, R_L = open, C_L = open, R_{CM} = open			180	mA
		Normal Mode (Recessive)	See Figure 5, TXD = V_{CC} or V_{IO}, R_L = 50 Ω, C_L = open, R_{CM} = open, STB = 0V		1.5	2.5	mA
		Standby Mode	Devices with the "V" suffix (I/O Level Shifting Devices), V_{CC} not needed in Standby Mode, See Figure 5, TXD = V_{IO}, R_L = 50 Ω, C_L = open, R_{CM} = open, STB = V_{IO}		0.5	5	µA
		Standby Mode	Devices without the "V" suffix (5V only), See Figure 5, TXD = V_{CC}, R_L = 50 Ω, C_L = open, R_{CM} = open, STB = V_{CC}			22	µA
I_{IO}	I/O Supply Current	Normal Mode	RXD floating, TXD = STB = 0 or 5.5 V		90	300	µA
		Standby Mode	RXD floating, TXD = STB = V_{IO}, V_{CC} = 0 or 5.5 V		12	17	µA
UV_{VCC}	Rising Undervoltage detection on V_{CC} for protected mode				4.2	4.4	V
	Falling Undervoltage detection on V_{CC} for protected mode			3.8	4.0	4.25	
$V_{HYS(UVVCC)}$	Hysteresis voltage on UV_{VCC}				200		mV
$UV_{(VIO)}$	Undervoltage detection on V_{IO} for protected mode		Devices with the "V" suffix (I/O Level Shifting Devices)	1.3		2.75	V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}		Devices with the "V" suffix (I/O Level Shifting Devices)		80		mV
STB TERMINAL (MODE SELECT INPUT)							
V_{IH}	HIGH-level input voltage		Devices with the "V" suffix (I/O Level Shifting Devices)	0.7 x V_{IO}			V
			Devices without the "V" suffix (5V only)	2			V
V_{IL}	LOW-level input voltage		Devices with the "V" suffix (I/O Level Shifting Devices)			0.3 x V_{IO}	V
			Devices without the "V" suffix (5V only)			0.8	V
I_{IH}	HIGH-level input leakage current		STB = V_{CC} = V_{IO} = 5.5 V	-2		2	µA
I_{IL}	Low-level input leakage current		STB = 0V, V_{CC} = V_{IO} = 5.5 V	–20	0	-2	µA
$I_{lkg(OFF)}$	Unpowered leakage current		STB = 5.5 V, V_{CC} = V_{IO} = 0 V	-1	0	1	µA
TXD TERMINAL (CAN TRANSMIT DATA INPUT)							
V_{IH}	HIGH level input voltage		Devices with the "V" suffix (I/O Level Shifting Devices)	0.7 x V_{IO}			V
			Devices without the "V" suffix (5V only)	2			
V_{IL}	LOW level input voltage		Devices with the "V" suffix (I/O Level Shifting Devices)			0.3 x V_{IO}	V
			Devices without the "V" suffix (5V only)			0.8	
I_{IH}	HIGH level input leakage current		TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low level input leakage current		TXD = 0V, V_{CC} = V_{IO} = 5.5 V	–100	-25	–7	µA
$I_{lkg(OFF)}$	Unpowered leakage current		TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 5 V, R_L = 60 Ω.

Electrical Characteristics (continued)

Over recommended operating conditions with T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
C_I	Input Capacitance				5		pF
RXD TERMINAL (CAN RECEIVE DATA OUTPUT)							
V_{OH}	HIGH level output voltage		Devices with the "V" suffix (I/O Level Shifting Devices), See Figure 6, I_O = –2 mA.	0.8 × V_{IO}			V
			Devices without the "V" suffix (5V only), See Figure 6, I_O = –2 mA.	4	4.6		
V_{OL}	LOW level output voltage		Devices with the "V" suffix (I/O Level Shifting Devices), See Figure 6, I_O = +2 mA.			0.2 x V_{IO}	
			Devices without the "V" suffix (5V only), See Figure 6, I_O = +2 mA.		0.2	0.4	
$I_{lkg(OFF)}$	Unpowered leakage current		RXD = 5.5 V, V_{CC} = 0 V, V_{IO} = 0 V	–1	0	1	µA
DRIVER ELECTRICAL CHARACTERISTICS							
$V_{O(D)}$	Bus output voltage (dominant)	CANH	See Figure 13 and Figure 5, TXD = 0 V, STB = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	2.75		4.5	V
		CANL		0.5		2.25	
$V_{O(R)}$	Bus output voltage (recessive)	CANH and CANL	See Figure 13 and Figure 5, TXD = V_{CC} or V_{IO}, V_{IO} = V_{CC}, STB = 0 V , R_L = open (no load), R_{CM} = open	2	0.5 × V_{CC}	3	
$V_{OD(D)}$	Differential output voltage (dominant)	CANH - CANL	See Figure 13 and Figure 5, TXD = 0 V, STB = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	1.5		3	
			See Figure 13 and Figure 5, TXD = 0 V, STB = 0 V, 45 Ω ≤ R_L < 50 Ω, C_L = open, R_{CM} = open	1.4		3	
$V_{OD(R)}$	Differential output voltage (recessive)	CANH - CANL	See Figure 13 and Figure 5, TXD = V_{CC}, STB = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	–120		12	mV
			See Figure 13 and Figure 5, TXD = V_{CC}, STB = 0 V, R_L = open (no load), C_L = open, R_{CM} = open	–50		50	
V_{SYM}	Output symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$ – $V_{O(CANL)}$)		See Figure 13 and Figure 5, STB at 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	–0.4		0.4	V
$I_{OS(SS\_DOM)}$	Short circuit steady-state output current, Dominant		See Figure 13 and Figure 11, STB at 0 V, V_{CANH} = 0 V, CANL = open, TXD = 0 V	–100			mA
			See Figure 13 and Figure 11, STB at 0 V, V_{CANL} = 32 V, CANH = open, TXD = 0 V			100	
$I_{OS(SS\_REC)}$	Short circuit steady-state output current, Recessive		See Figure 13 and Figure 11, STB at 0 V, –20 V ≤ V_{BUS} ≤ 32 V, Where V_{BUS} = CANH = CANL, TXD = V_{CC}, Normal Mode	–5		5	mA
RECEIVER ELECTRICAL CHARACTERISTICS							
CM	Common mode range, normal mode		See Figure 6 and Table 1, STB = 0 V	-30		+30	V
V_{IT+}	Positive-going input threshold voltage, normal mode		See Figure 6, Table 6 and Table 1, STB = 0 V, -20 V ≤ CM ≤ +20 V			900	mV
$V_{IT–}$	Negative-going input threshold voltage, normal mode			500			
V_{IT+}	Positive-going input threshold voltage, normal mode		See Figure 6, Table 6 and Table 1, STB = 0 V, -30 V ≤ CM ≤ +30 V			1000	
$V_{IT–}$	Negative-going input threshold voltage, normal mode			400			
V_{HYS}	Hysteresis voltage (V_{IT+} - $V_{IT–}$), normal mode		See Figure 6, Table 6 and Table 1, STB = 0 V		120		

Electrical Characteristics (continued)

Over recommended operating conditions with T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
CM	Common mode range, standby mode	Devices with the "V" suffix (I/O Level Shifting Devices), See Figure 6, Table 6 and Table 1, STB = V_{IO}, 4.5 V ≤ V_{IO} ≤ 5.5 V	-12		12	V
		Devices with the "V" suffix (I/O Level Shifting Devices), See Figure 6, Table 6 and Table 1, STB = V_{IO}, 3.0 V ≤ V_{IO} ≤ 4.5 V	-2		+7	
		Devices without the "V" suffix (5V only), See Figure 6, Table 6 and Table 1, STB = V_{CC}	-12		12	
$V_{IT(STANDBY)}$	Input threshold voltage, standby mode	STB = V_{CC} or V_{IO}	400		1150	mV
$I_{LKG(IOFF)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = 0 V			6	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{CC}, V_{IO} = V_{CC}, V_I = 0.4 sin (4E6 π t) + 2.5 V		24	30	pF
C_{ID}	Differential input capacitance (CANH to CANL)	TXD = V_{CC}, V_{IO} = V_{CC}, V_I = 0.4 sin (4E6 π t)		12	15	
R_{ID}	Differential input resistance	TXD = V_{CC} = V_{IO} = 5 V, STB = 0 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)		15		40	
$R_{IN(M)}$	Input resistance matching: [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$	–2%		2%	

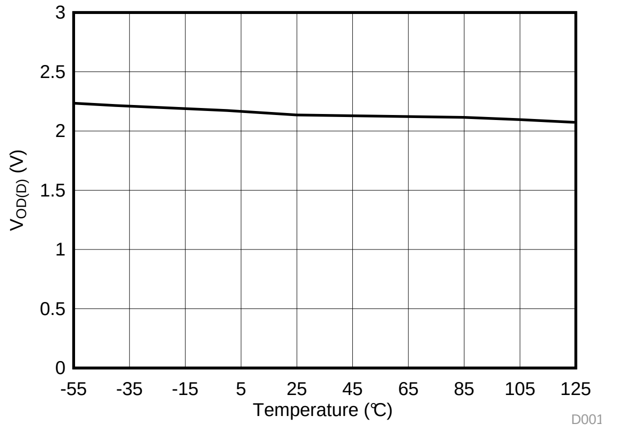
7.6 Switching Characteristics

Over recommended operating conditions with T_A = -55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See Figure 8, STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		100	160	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive			110	175	
t_{MODE}	Mode change time, from Normal to Standby or from Standby to Normal	See Figure 7		1	45	µs
t_{WK_FILTER}			0.5		1.85	
DRIVER SWITCHING CHARACTERISTICS						
t_{pHR}	Propagation delay time, HIGH TXD to Driver Recessive	See Figure 5, STB = 0 V, R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		75		ns
t_{pLD}	Propagation delay time, LOW TXD to Driver Dominant			55		
$t_{sk(p)}$	Pulse skew (|t_{pHR} - t_{pLD}|)			20		
t_R	Differential output signal rise time			45		
t_F	Differential output signal fall time			45		
t_{TXD_DTO}	Dominant timeout(2)	See Figure 10, STB = 0 V, R_L = 60 Ω, C_L = open	1.2		3.8	ms
RECEIVER SWITCHING CHARACTERISTICS						
t_{pRH}	Propagation delay time, bus recessive input to high output	See Figure 6, STB = 0 V, $C_{L(RXD)}$ = 15 pF		65		ns
t_{pDL}	Propagation delay time, bus dominant input to low output			50		ns
t_R	RXD Output signal rise time			10		ns
t_F	RXD Output signal fall time			10		ns
FD Timing Parameters						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns, all devices	See Figure 9 , STB = 0 V, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns, G device variants only		155		210	
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns, all devices		400		550	
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns, G device variants only		120		220	
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns, all devices		-65		40	
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns, G device variants only		-45		15	

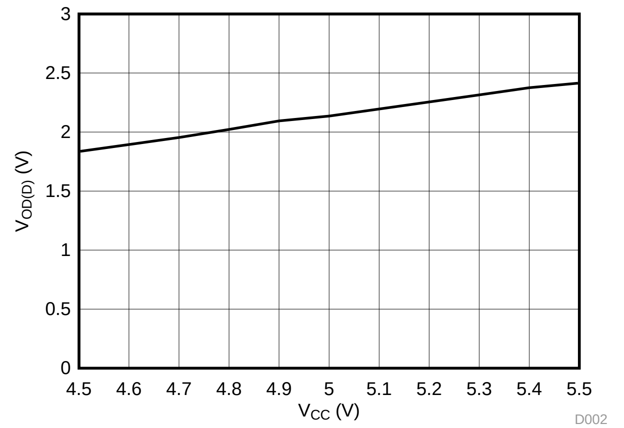
(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 5 V, R_L = 60 Ω.
(2) The TXD dominant timeout ($t_{(TXD\_DTO)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(TXD\_DTO)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(TXD\_DTO)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11 / $t_{(TXD\_DTO)}$

7.7 Typical Characteristics



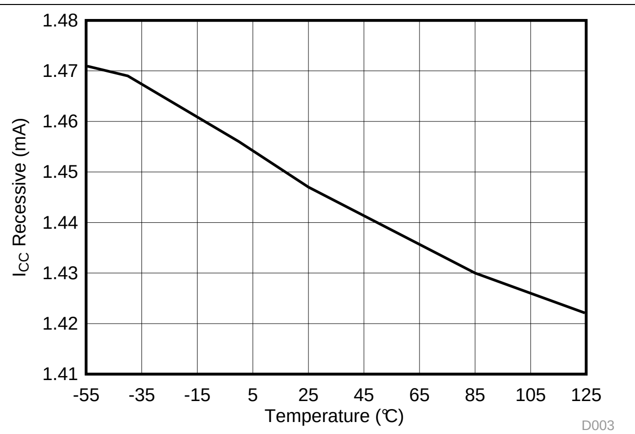
V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω
C_L = Open RCM = Open STB = 0 V

Figure 1. $V_{OD(D)}$ over Temperature



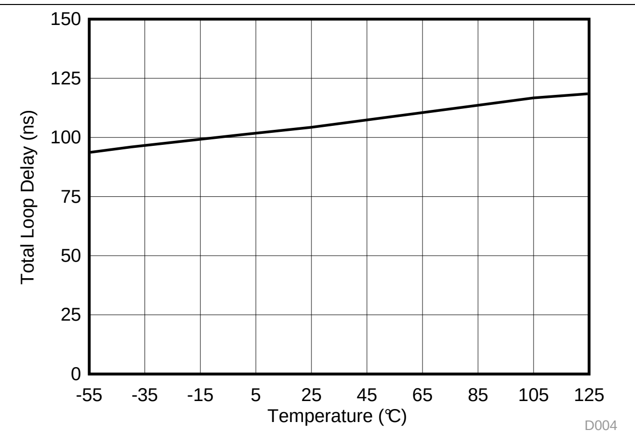
V_{IO} = 5 V STB = 0 V R_L = 60 Ω
C_L = Open RCM = Open Temp = 25°C

Figure 2. $V_{OD(D)}$ over V_{CC}



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω
C_L = Open RCM = Open STB = 0 V

Figure 3. I_{CC} Recessive over Temperature



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω
C_L = 100 pF C_{L_RXD} = 15 pF STB = 0 V

Figure 4. Total Loop Delay over Temperature

8 Parameter Measurement Information

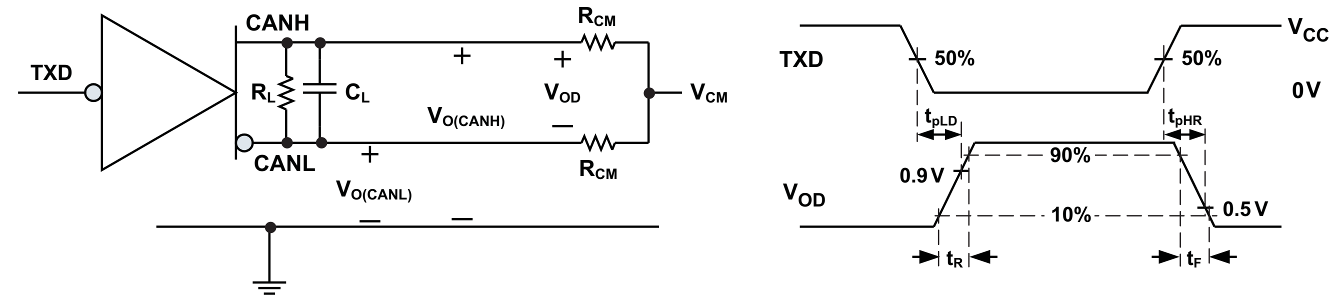


Figure 5. Driver Test Circuit and Measurement

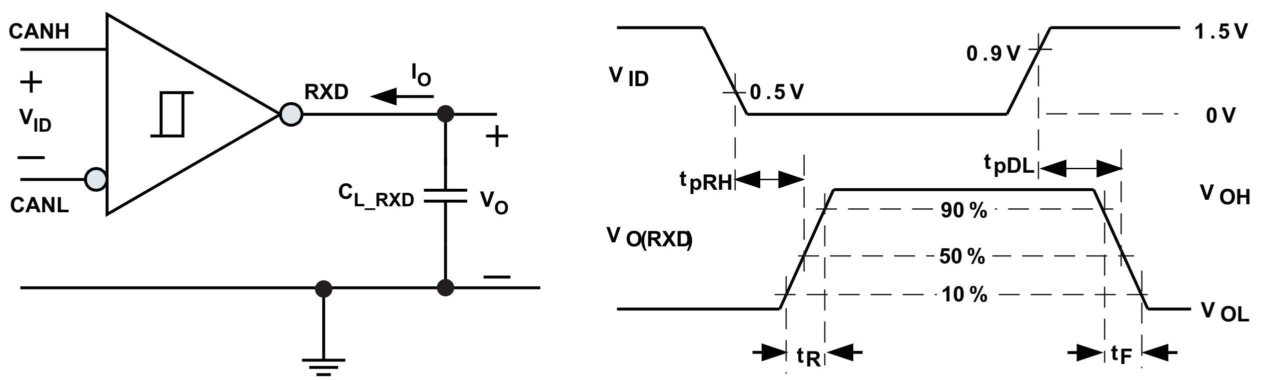


Figure 6. Receiver Test Circuit and Measurement

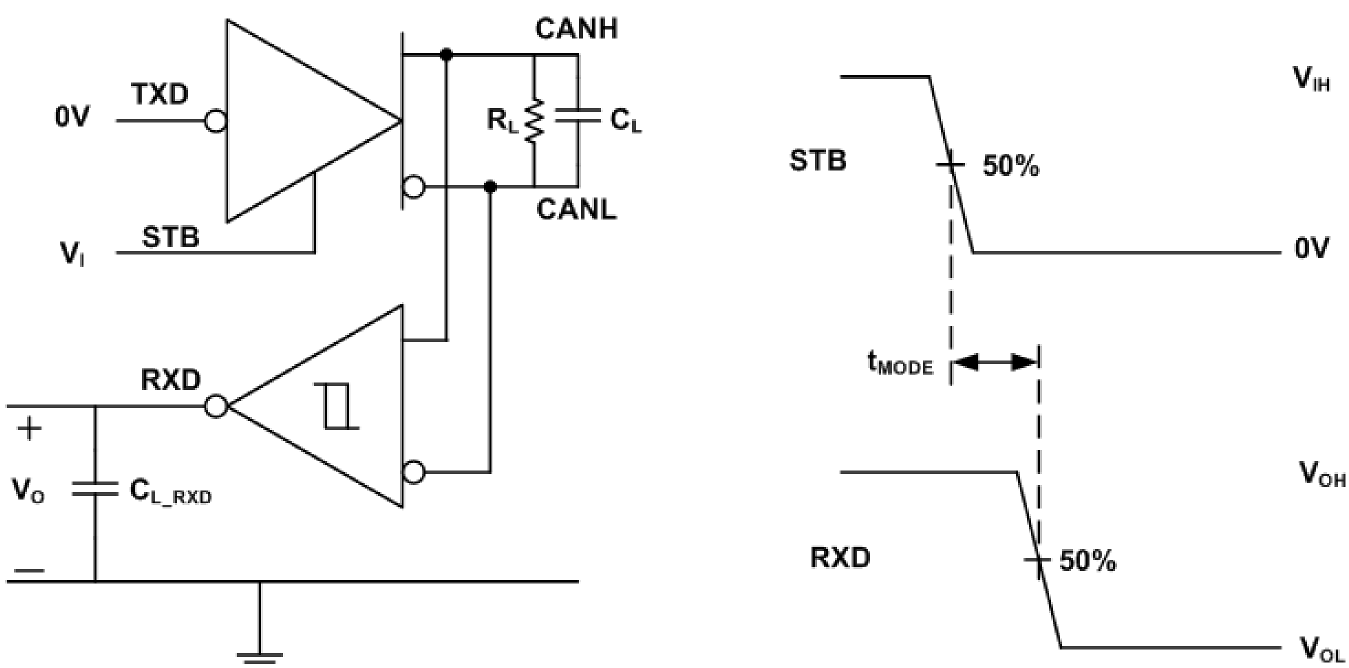


Figure 7. t_{MODE} Test Circuit and Measurement

Parameter Measurement Information (continued)

Table 1. Receiver Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\|V_{ID}\|$	RXD	
-29.5	-30.5	1000 mV	L	V_{OL}
30.5	29.5	1000 mV	L	
-19.55	-20.45	900 mV	L	
20.45	19.55	900 mV	L	
-19.75	-20.25	500 mV	H	V_{OH}
20.25	19.75	500 mV	H	
-29.8	-30.2	400 mV	H	
30.2	29.8	400 mV	H	
Open	Open	X	H	

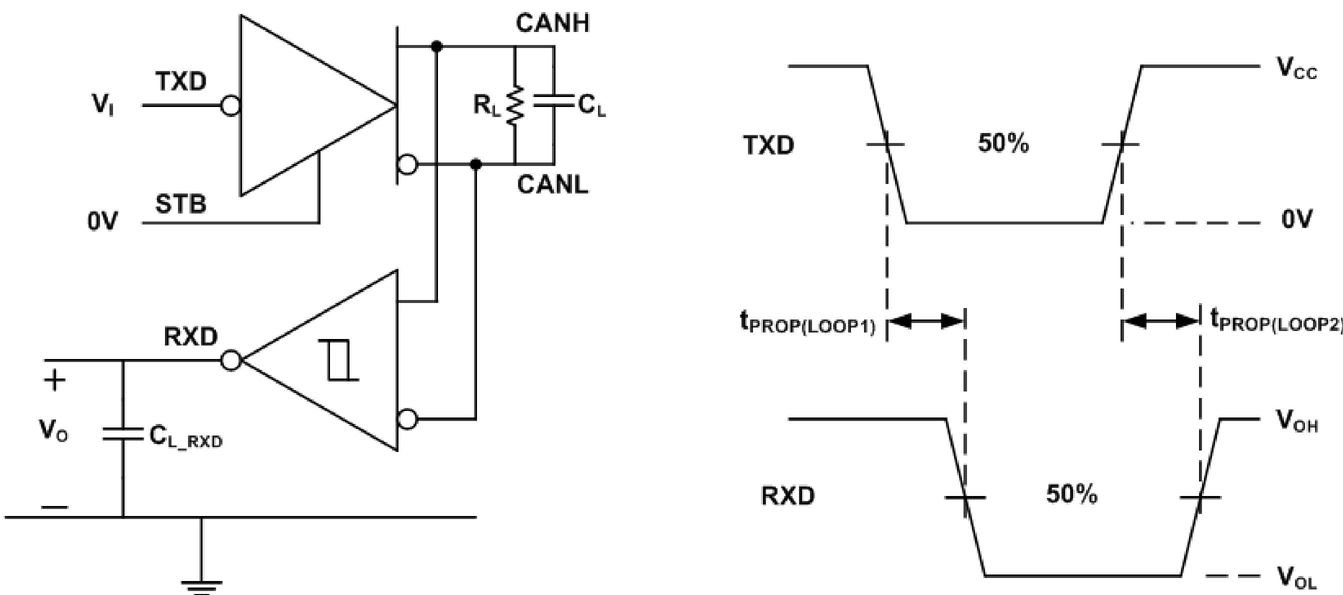


Figure 8. $T_{PROP(LOOP)}$ Test Circuit and Measurement

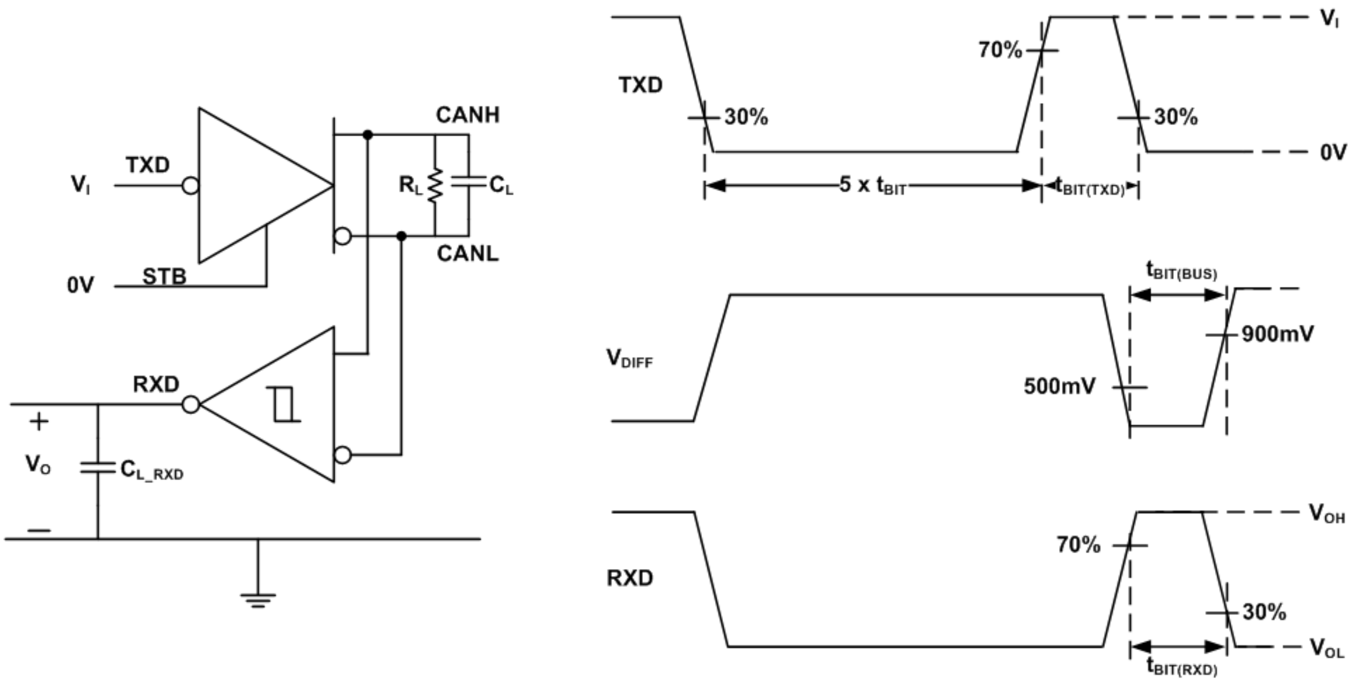


Figure 9. CAN FD Timing Parameter Measurement

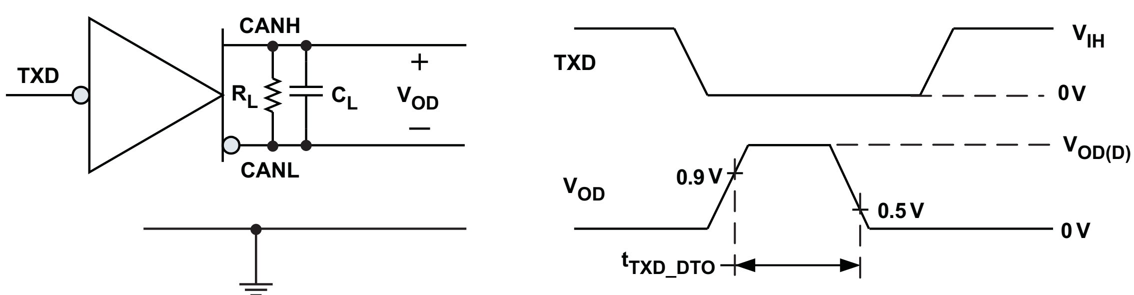


Figure 10. TXD Dominant Timeout Test Circuit and Measurement

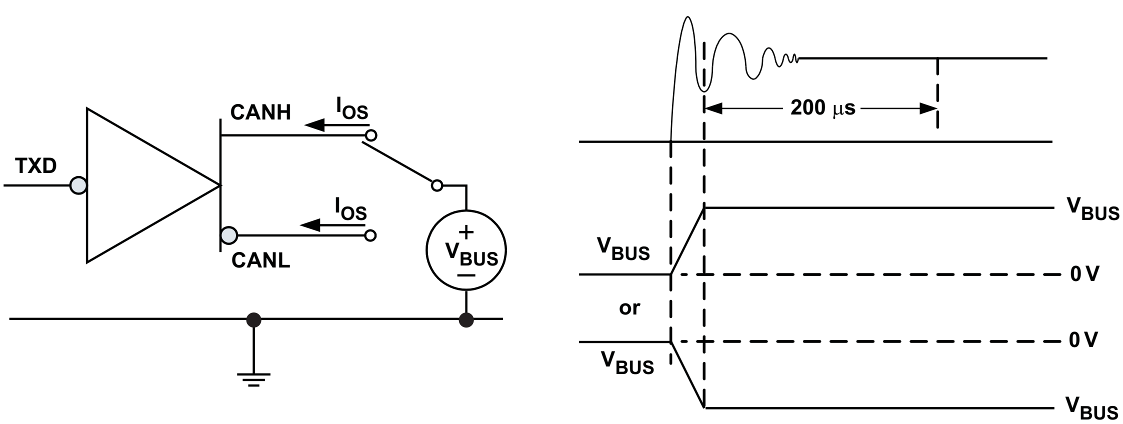


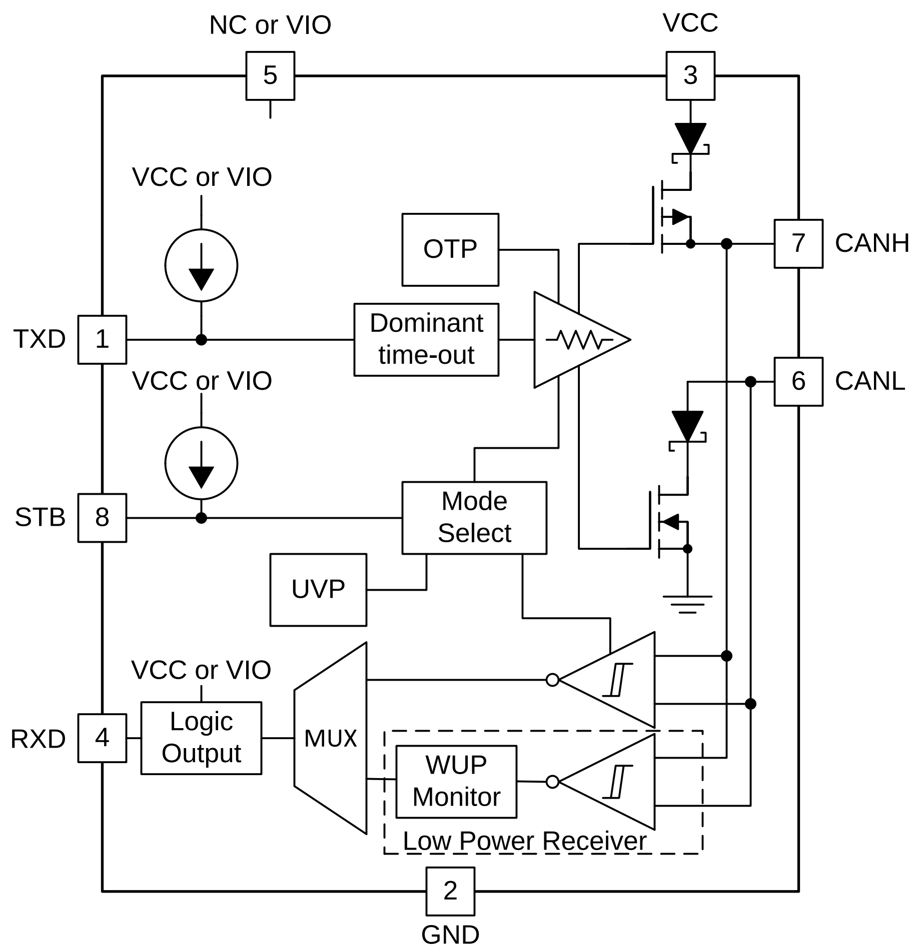
Figure 11. Driver Short Circuit Current Test and Measurement

9 Detailed Description

9.1 Overview

These CAN transceivers meet the ISO1189-2 (2016) High Speed CAN (Controller Area Network) physical layer standard. They are designed for data rates in excess of 1 Mbps for CAN FD, and enhanced timing margin / higher data rates in long and highly-loaded networks. These devices provide many protection features to enhance device and CAN-network robustness.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 TXD Dominant Timeout (DTO)

During normal mode (the only mode where the CAN driver is active), the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The DTO circuit timer starts on a falling edge on TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen before the timeout period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on the TXD terminal, thus clearing the TXD DTO condition. The receiver and RXD terminal still reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during a TXD dominant timeout.

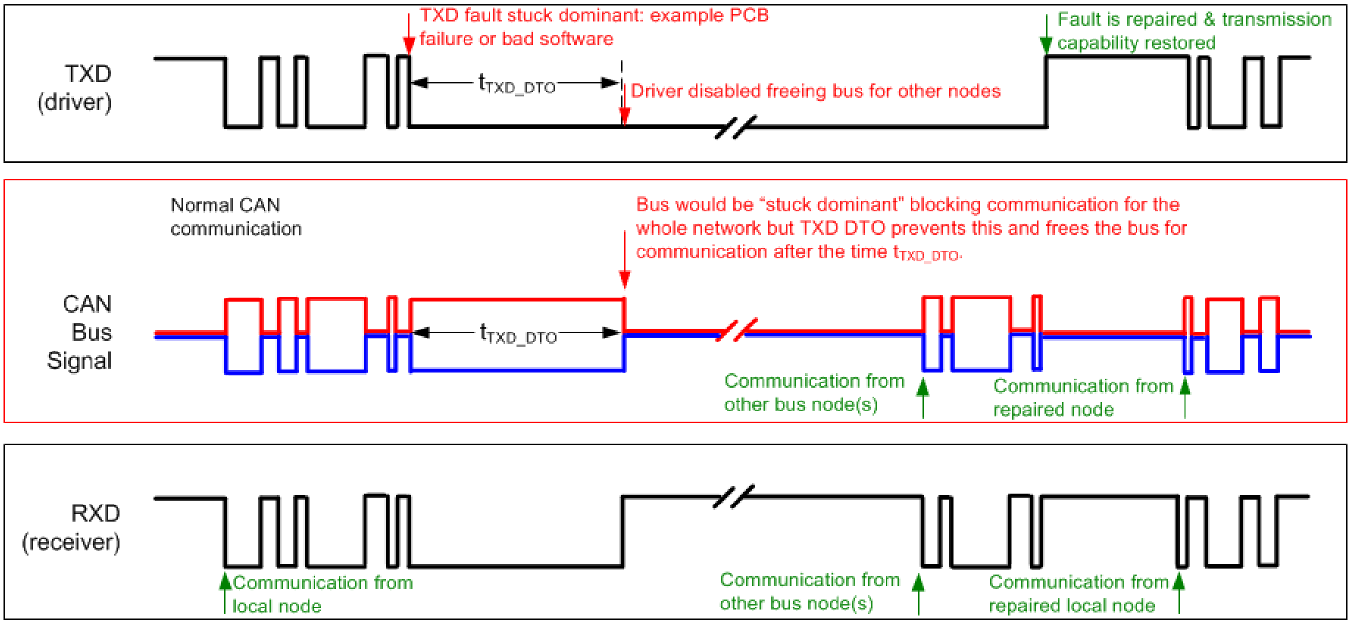


Figure 12. Example Timing Diagram for TXD DTO

NOTE

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate by: Minimum Data Rate = 11 / t_{TXD_DTO}.

9.3.2 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold, the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device.

NOTE

During thermal shutdown the CAN bus drivers turn off; thus no transmission is possible from TXD to the bus. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver to RXD path remains operational.

Feature Description (continued)

9.3.3 Undervoltage Lockout

The supply terminals have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the V_{CC} or V_{IO} supply terminals.

Table 2. Undervoltage Lockout 5 V Only Devices (Devices without the "V" Suffix)(1)

V_{CC}	DEVICE STATE	BUS OUTPUT	RXD
GOOD	Normal	Per Device State and TXD	Mirrors Bus
BAD	Protected	High Impedance	High Impedance (3-state)

(1) See the V_{IT} section of the *Electrical Characteristics*.

Table 3. Undervoltage Lockout I/O Level Shifting Devices (Devices with the "V" Suffix)

V_{CC}	V_{IO}	DEVICE STATE	BUS OUTPUT	RXD
GOOD	GOOD	Normal	Per STB and TXD	Mirrors Bus
BAD	GOOD	Protected	High Impedance	High (Recessive)
GOOD	BAD	Protected	Recessive	High Impedance (3-state)
BAD	BAD	Protected	High Impedance	High Impedance (3-state)

NOTE

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation within 300 µs.

9.3.4 Unpowered Device

The device is designed to be an 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered so they will not load down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

9.3.5 Floating Terminals

These devices have internal pull ups on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to V_{CC} or V_{IO} to force a recessive input level if the terminal floats. The STB terminal is also pulled up to force the device into low power standby mode if the terminal floats.

9.3.6 CAN Bus Short Circuit Current Limiting

The device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include driver current limiting (dominant and recessive). The device has TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states with the data and control fields bits, thus the short circuit current may be viewed either as the instantaneous current during each bus state, or as a DC average current. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit stuffing
- Interframe space
- TXD dominant time out (fault case limiting)

These ensure a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

NOTE

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with the following formula:

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}] \quad (1)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

NOTE

Consider the short circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

9.3.7 Digital Inputs and Outputs

9.3.7.1 5 V V_{CC} Only Devices (Devices without the "V" Suffix):

The 5 V V_{CC} only devices are supplied by a single 5 V rail. The digital inputs have TTL input thresholds and are therefore 5 V and 3.3 V compatible. The RXD outputs on these devices are driven to the V_{CC} rail for logic high output. Additionally, the TXD and STB pins are internally pulled up to V_{CC}.

NOTE

TXD and STB are internally pulled up to V_{CC}. However, the internal bias may only put the device into a known state if the terminals float. The internal bias may be inadequate for system-level biasing. TXD pull up strength and CAN bit timing require special consideration when these devices are used with CAN controllers with an open-drain TXD output. An adequate external pull up resistor must be used to ensure that the CAN controller output of the micrcontroller maintains adequate bit timing to the TXD input.

9.3.7.2 5 V V_{CC} with V_{IO} I/O Level Shifting (Devices with the "V" Suffix):

These devices use a 5 V V_{CC} power supply for the CAN driver and high speed receiver blocks. These transceivers have a second separate supply for I/O level shifting (V_{IO}). This supply is used to set the CMOS input thresholds of the TXD and STB pins and the RXD high level output voltage. The internal pull ups on TXD and STB are weakly pulled up to V_{IO}.

9.4 Device Functional Modes

The device has two main operating modes: normal mode and standby mode. Operating mode selection is made via the STB input terminal.

Table 4. Operating Modes

STB Terminal	MODE	DRIVER	RECEIVER	RXD Terminal
LOW	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State (1)
HIGH	Standby Mode	Disabled (OFF)	Disabled (OFF) (Low Power Bus Monitor is Active)	High (Unless valid WUP has been received)

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

9.4.1 Can Bus States

The CAN bus has two states during powered operation of the device; *dominant* and *recessive*. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD terminal. A recessive bus state is when the bus is biased to V_{CC} / 2 via the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the TXD and RXD terminals. See Figure 13 and Figure 14.

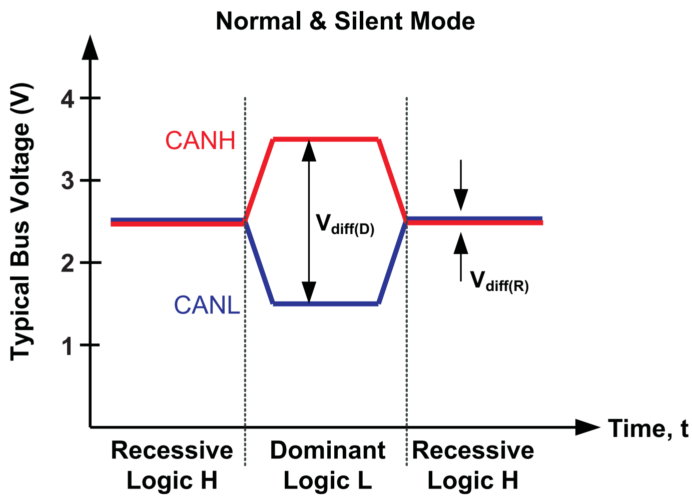


Figure 13. Bus States (Physical Bit Representation)

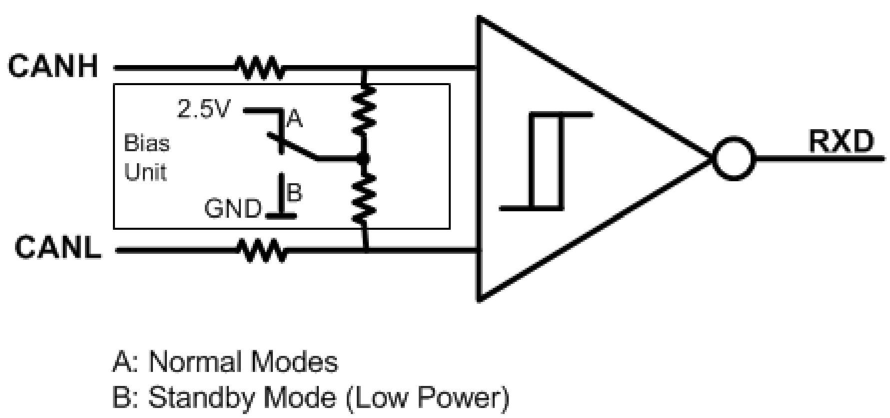


Figure 14. Bias Unit (Recessive Common Mode Bias) and Receiver

9.4.2 Normal Mode

Select the *normal mode* of device operation by setting STB low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

9.4.3 Standby Mode

Activate low power *standby mode* by setting STB high. The CAN driver and high speed receiver are turned off to save system power. A low power receiver remains active to monitor the bus for a valid wake up pattern (WUP). The RXD output will remain high until a valid WUP has been received.

9.4.3.1 Remote Wake Request via Wake Up Pattern (WUP) in Standby Mode

The TCAN1042 family offers a remote wake request feature that is used to indicate to the host micrcontroller that the bus is active and the node should return to normal operation.

These devices use the multiple filtered dominant wake up pattern (WUP) from the ISO11898-2 (2016) to qualify bus activity. Once a valid WUP has been received the wake request will be indicated to the micrcontroller by a falling edge and low corresponding to a "filtered" dominant on the RXD output terminal.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. These filtered dominant, recessive, dominant pulses do not need to occur in immediate succession. There is no timeout that will occur between filtered bits of the WUP. Once a full WUP has been detected the device will continue to drive the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive signal to be considered "filtered", the bus must continually remain in that state for more than t_{WK_FILTER}. Due to variability in the t_{WK_FILTER}, the following three scenarios can exist:

1. Bus signals that last less than $t_{WK\_FILTER(MIN)}$ will never be detected as part of a valid WUP
2. Bus signals that last more than $t_{WK\_FILTER(MIN)}$ but less than $t_{WK\_FILTER(MAX)}$ may be detected as part of a valid WUP
3. Bus signals that last more than $t_{WK\_FILTER(MAX)}$ will always be detected as part of a valid WUP

Once the first filtered dominant signal is received, the device is now waiting on a filtered recessive signal, other bus traffic will not reset the bus monitor. Once the filtered recessive signal is received, the monitor is now waiting on a second filtered dominant signal, and again other bus traffic will not reset the monitor. After reception of the full WUP, the device will transition to driving the RXD output pin low for the remainder of any dominant signal that remains on the bus for longer than t_{WK_FILTER}.

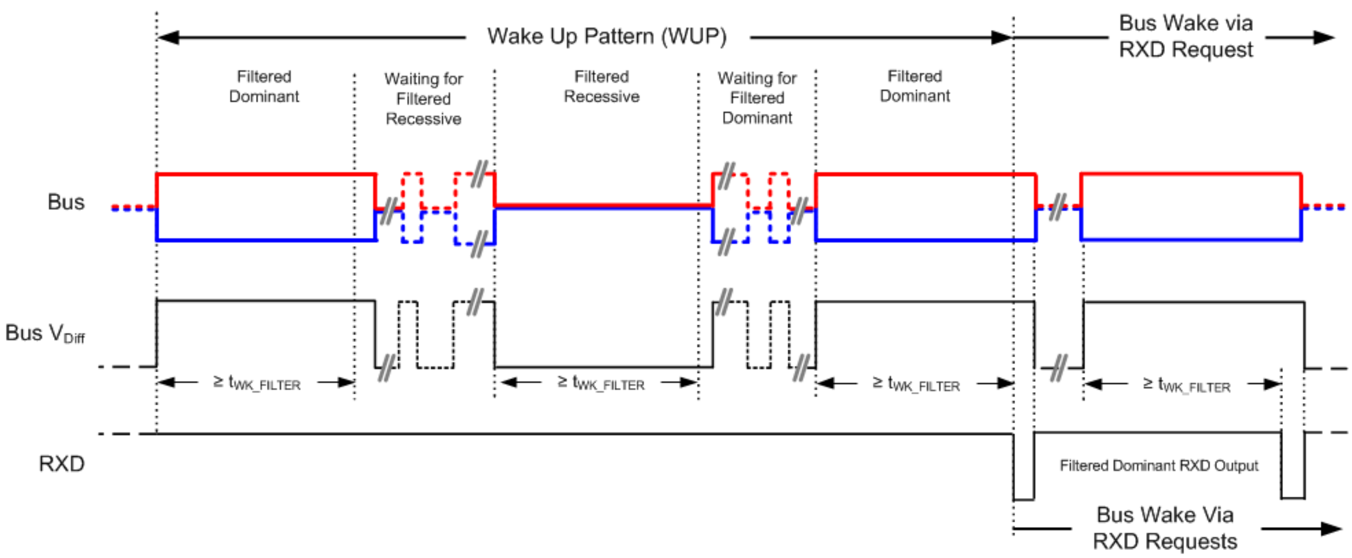


Figure 15. Wake Up Pattern (WUP)

9.4.4 Driver and Receiver Function Tables

Table 5. Driver Function Table

DEVICE	INPUTS		OUTPUTS		DRIVEN BUS STATE
	STB (1) (2)	TXD (1) (3)	CANH (1)	CANL (1)	
All Devices	L	L	H	L	Dominant
		H or Open	Z	Z	Recessive
	H or Open	X	Z	Z	Recessive

(1) H = high level, L = low level, X= irrelevant, Z = common mode (recessive) bias to V_{CC} / 2. See Figure 13 and Figure 14 for bus state and common mode bias information.
(2) Devices have an internal pull up to V_{CC} or V_{IO} on STB terminal. If STB terminal is open the terminal will be pulled high and the device will be in standby mode.
(3) Devices have an internal pull up to V_{CC} or V_{IO} on TXD terminal. If the TXD terminal is open the terminal will be pulled high and the transmitter will remain in recessive (non-driven) state.

Table 6. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD TERMINAL (1)
Normal or Silent	$V_{ID} \geq 0.9$ V	Dominant	L (2)
	0.5 V < V_{ID} < 0.9 V	?	? (2)
	$V_{ID} \leq 0.5$ V	Recessive	H (2)
	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level, ? = indeterminate.
(2) See Receiver Electrical Characteristics section for input thresholds.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Below are typical application configurations for both 5 V and 3.3 V microprocessor applications. The bus termination is shown for illustrative purposes.

10.2 Typical Applicationspurposes. Typical

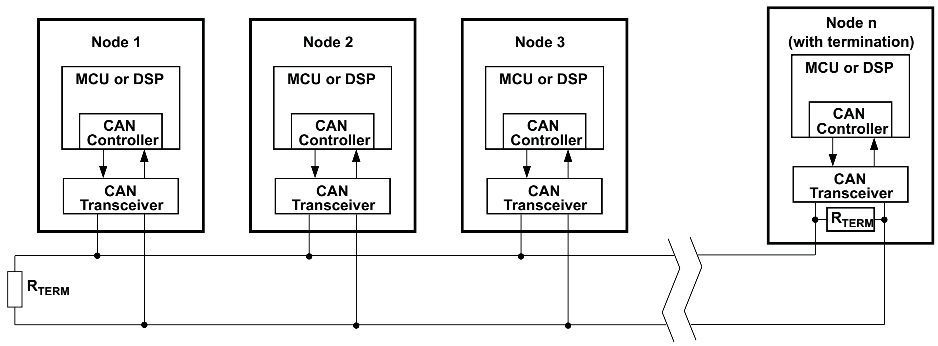


Figure 16. Typical 5 V Application

10.2.1 Design Requirements

10.2.1.1 Bus Loading, Length and Number of Nodes

The ISO11898 Standard specifies a maximum bus length of 40m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TCAN1042 family of transceivers.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898. They have made system level trade offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet and NMEA2000.

A CAN network design is a series of tradeoffs, but these devices operate over wide common-mode range. In ISO11898-2 the driver differential output is specified with a 60 Ω load (the two 120 Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The TCAN1042 family is specified to meet the 1.5 V requirement with a 50Ω load incorporating the worst case including parallel transceivers. The differential input resistance of the TCAN1042 family is a minimum of 30 kΩ. If 100 TCAN1042 family transceivers are in parallel on a bus, this is equivalent to a 300Ω differential load worst case. That transceiver load of 300 Ω in parallel with the 60Ω gives an equivalent loading of 50 Ω. Therefore, the TCAN1042 family theoretically supports up to 100 transceivers on a single bus segment with margin to the 1.2 V minimum differential input at each node. However for CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO11898 standard of 40m by careful system design and datarate tradeoffs. For example CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO11898 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

Typical Applicationspurposes. Typical (continued)

10.2.2 Detailed Design Procedures

10.2.2.1 Can Termination

The ISO11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network.

Termination may be a single 120 Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. (See Figure 17). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

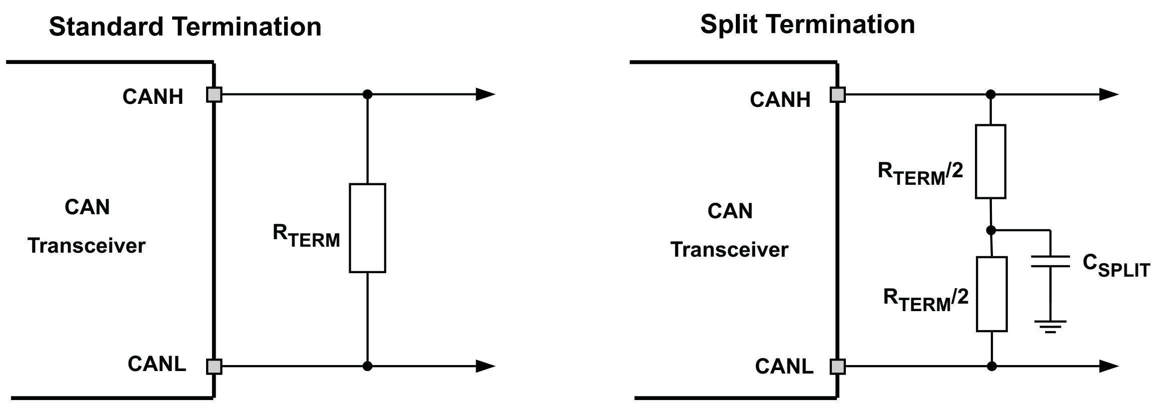


Figure 17. CAN Bus Termination Concepts

The TCAN1042 family of transceivers have variants for both 5 V only applications and applications where level shifting is needed for a 3.3 V micrcontroller.

Typical Applicationspurposes. Typical (continued)

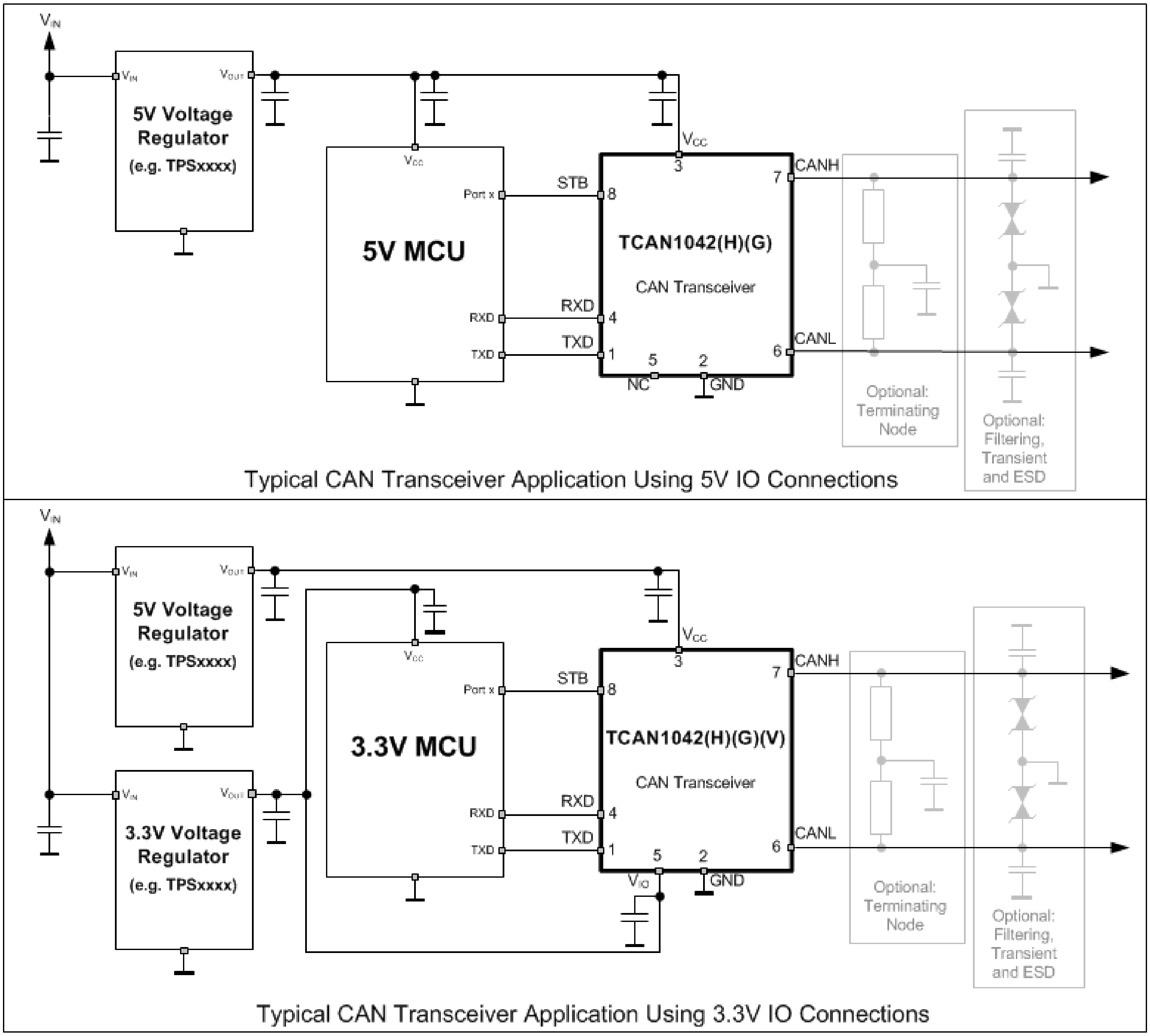
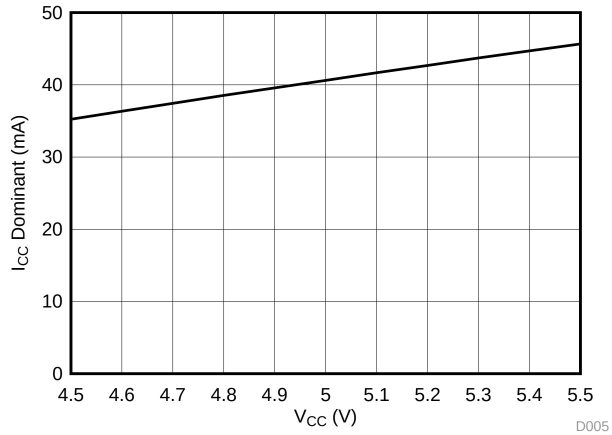


Figure 18. Typical CAN Bus

Typical Applicationspurposes. Typical (continued)

10.2.3 Application Curves



V_{CC} = 4.5 V to 5.5 V	V_{IO} = 3.3 V	R_L = 60 Ω
C_L = Open	Temp = 25°C	STB = 0 V

Figure 19. I_{CC} Dominant Current over V_{CC} Supply Voltage

11 Power Supply Requirements

These devices are designed to operate from main V_{CC} input voltage supply range between 4.5 V and 5.5 V. Some devices have an output level shifting supply input, V_{IO}, designed for a range between 3.0 V and 5.5 V. Both supply inputs must be well regulated. A bulk capacitance, typically 4.7 µF, should be placed near the CAN transceiver's main V_{CC} supply terminal in addition to bypass capacitors. A bulk capacitance, typically 1 µF, should be placed near the CAN transceiver's V_{IO} supply terminal in addition to bypass capacitors.

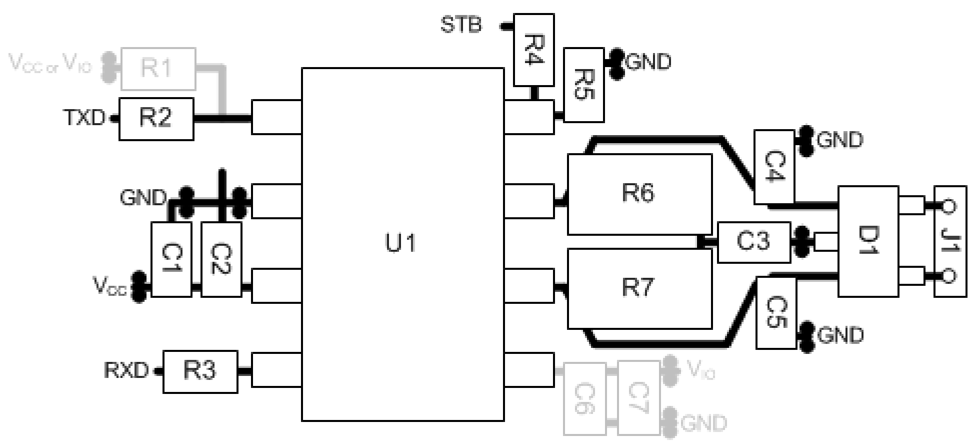
12 Layout

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. The TCAN1042 family comes with high on chip IEC ESD protection but if higher levels of system level immunity are desired, external TVS diodes can be used. TVS diodes and bus filtering capacitors should be placed as close to the on board connectors as possible to prevents noisy transient events from propagating further into the PCB and system.

12.1 Layout Guidelines

- Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from penetrating onto the board. In this layout example for protection a Transient Voltage Suppression (TVS) device, D1, has been used. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C4 and C5. Additionally (not shown) a series optional Common Mode Choke (CMC) can be placed on the CANH and CANL lines between the transceiver U1 and connector J1.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use supply (V_{CC}) and ground planes to provide low inductance. Note: high frequency current follows the path of least inductance and not the path of least resistance.
- Use at least two vias for supply (V_{CC}) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples C1, C2 (V_{CC}).
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R6 and R7, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination. See the application section for information on power ratings needed for the termination resistor(s).
- To limit current of digital lines, serial resistors may be used. Examples are R2, R3, and R4. These are not required.
- Terminal 1: R1 is shown optionally for the TXD input of the device. If an open drain host processor is used, this is mandatory to ensure the bit timing into the device is met.
- Terminal 5: For "V" variants of the TCAN1042 family, bypass capacitors should be placed as close to the pin as possible (example C6 and C7). For device options without V_{IO} I/O level shifting, this pin is not internally connected and can be left floating or tied to any existing net, for example a split pin connection.
- Terminal 8: is shown assuming the mode terminal, STB, will be used. If the device will only be used in normal mode, R4 is not needed and R5 could be used for the pull down resistor to GND.

12.2 Layout Example



13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TCAN1042-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1042V-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1042H-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1042HV-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1042G-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1042GV-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1042HG-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1042HGV-Q1	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

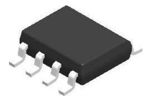
13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

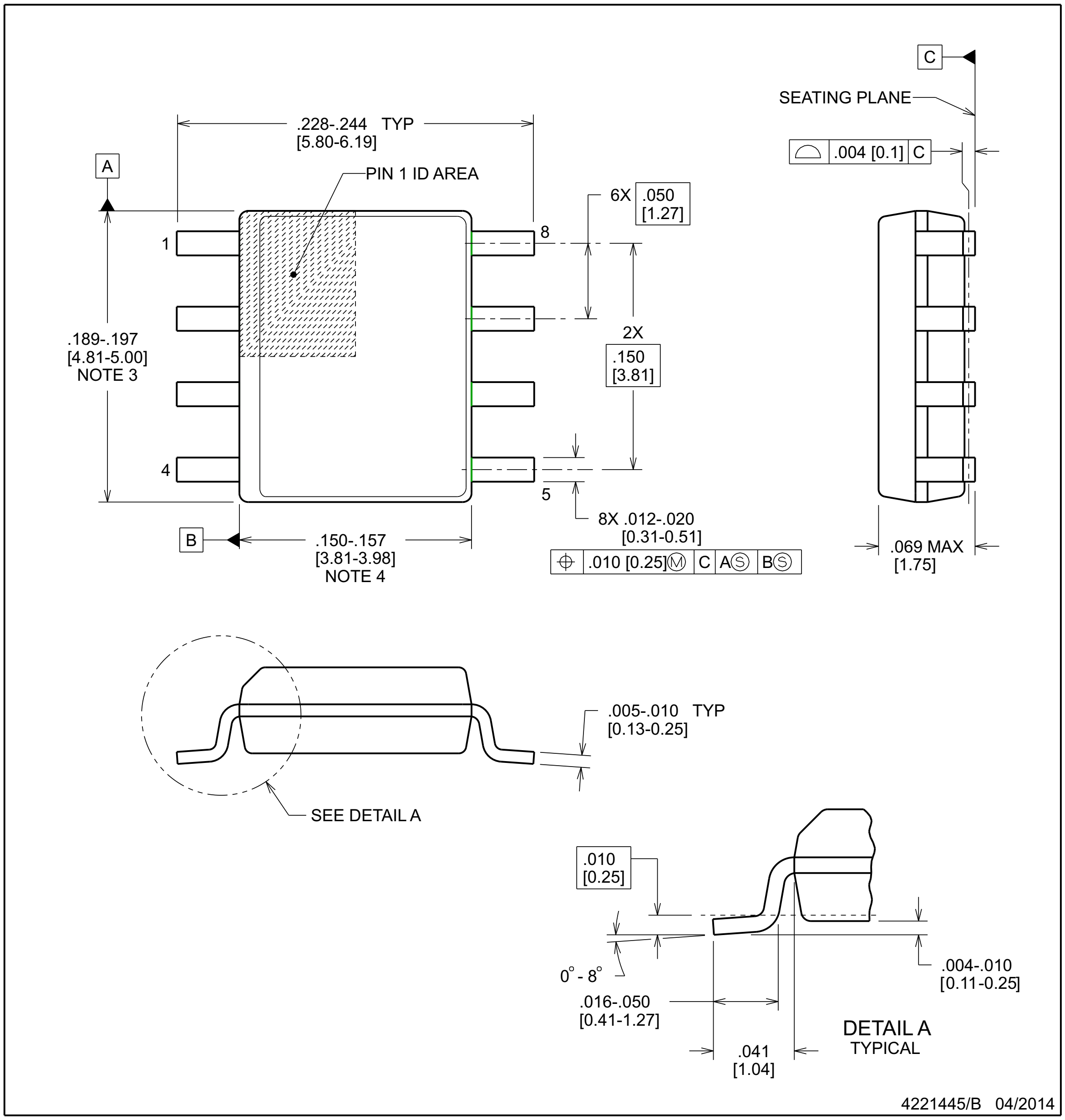


PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES:

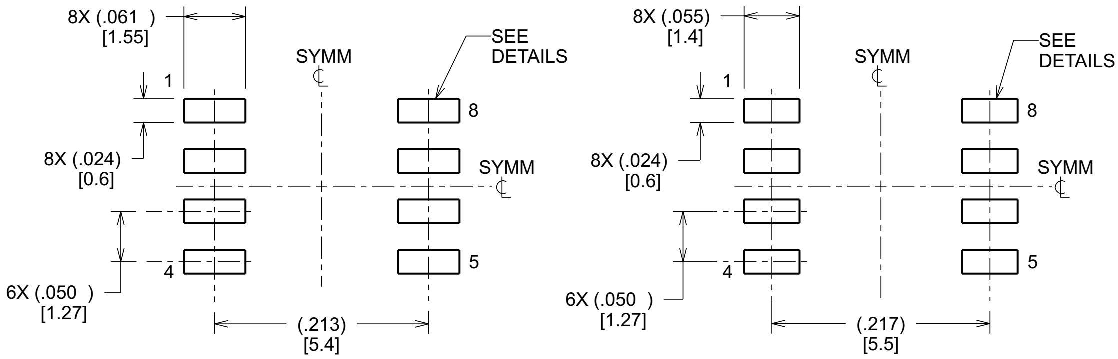
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

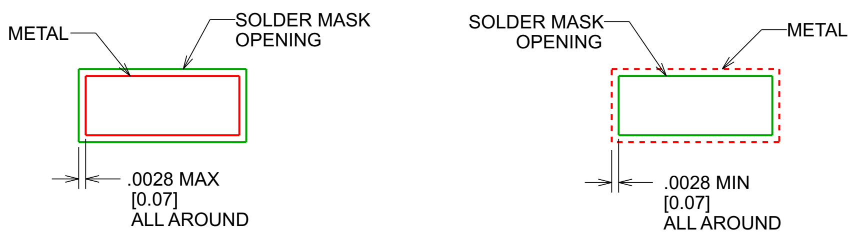
SOIC



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/B 04/2014

NOTES: (continued)

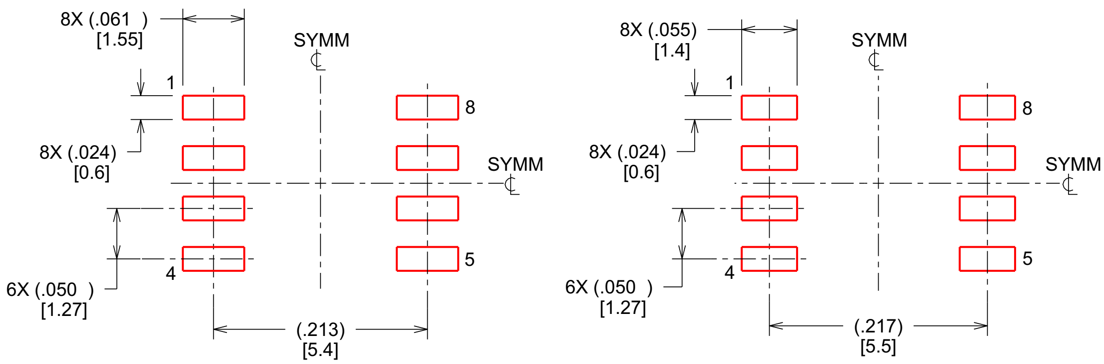
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SOIC



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/B 04/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1042DQ1	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-55 to 125		
TCAN1042DRQ1	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-55 to 125		
TCAN1042GDQ1	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-55 to 125		
TCAN1042GDRQ1	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-55 to 125		
TCAN1042GVDQ1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V	Samples
TCAN1042GVDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V	Samples
TCAN1042HDQ1	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-55 to 125		
TCAN1042HDRQ1	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-55 to 125		
TCAN1042HGDQ1	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-55 to 125		
TCAN1042HGDRQ1	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-55 to 125		
TCAN1042HGVDQ1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V	Samples
TCAN1042HGVDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V	Samples
TCAN1042HVDQ1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V	Samples
TCAN1042HVDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V	Samples
TCAN1042VDQ1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V	Samples
TCAN1042VDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1042V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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