

NTD5865NL

N-Channel Power MOSFET 60 V, 40 A, 16 mΩ

Features

- Low Gate Charge
- Fast Switching
- High Current Capability
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	60	V
Gate-to-Source Voltage - Continuous	V_{GS}	± 20	V
Gate-to-Source Voltage - Non-Repetitive ($t_p < 10 \mu\text{s}$)	V_{GS}	± 30	V
Continuous Drain Current ($R_{\theta JC}$)	Steady State	$T_C = 25^\circ\text{C}$	I_D 40 A
		$T_C = 100^\circ\text{C}$	26
Power Dissipation ($R_{\theta JC}$)	Steady State	$T_C = 25^\circ\text{C}$	P_D 52 W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	137 A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	40	A
Single Pulse Drain-to-Source Avalanche Energy	(L = 0.1 mH)	E_{AS}	36 mJ
		I_{AS}	27 A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.4	$^\circ\text{C/W}$
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	42	

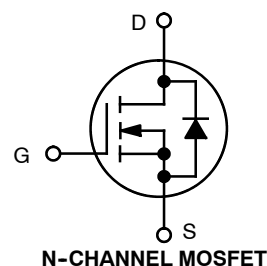
1. Surface-mounted on FR4 board using 1 in sq pad size
(Cu area = 1.127 in sq [2 oz] including traces).



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<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on) MAX}$	$I_D MAX$
60 V	16 mΩ @ 10 V	40 A
	19 mΩ @ 4.5 V	



N-CHANNEL MOSFET

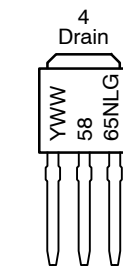
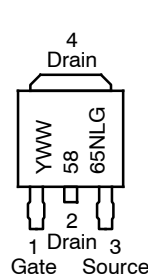


DPAK
CASE 369AA
(Surface Mount)
STYLE 2



IPAK
CASE 369D
(Straight Lead)
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENT



Y = Year
WW = Work Week
5865NL = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NTD5865NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			55		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$			1.0	μA
		$T_J = 25^\circ\text{C}$				
		$T_J = 150^\circ\text{C}$			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.6		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		13	16	m Ω
Drain-to-Source on Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		16	19	m Ω
Forward Transconductance	gFS	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		15		S

CHARGES, CAPACITANCES AND GATE RESISTANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		1400		pF
Output Capacitance	C_{oss}			137		
Reverse Transfer Capacitance	C_{rss}			95		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 40\text{ A}$		29		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.1		
Gate-to-Source Charge	Q_{GS}			4		
Gate-to-Drain Charge	Q_{GD}			8		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 40\text{ A}$		15		nC
Gate Resistance	R_G			1.3		Ω

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 48\text{ V}, I_D = 40\text{ A}, R_G = 2.5\text{ }\Omega$		8.4		ns
Rise Time	t_r			12.4		
Turn-Off Delay Time	$t_{d(off)}$			26		
Fall Time	t_f			4.4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 40\text{ A}$	$T_J = 25^\circ\text{C}$		0.95	1.2	V
			$T_J = 125^\circ\text{C}$		0.85		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di/dt = 100\text{ A}/\mu\text{s}, I_S = 40\text{ A}$		20		ns	
Charge Time	t_a			13			
Discharge Time	t_b			7			
Reverse Recovery Charge	Q_{RR}			13			nC

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

3. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Order Number	Package	Shipping [†]
NTD5865NL-1G	IPAK (Straight Lead) (Pb-Free)	75 Units / Rail
NTD5865NLT4G	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

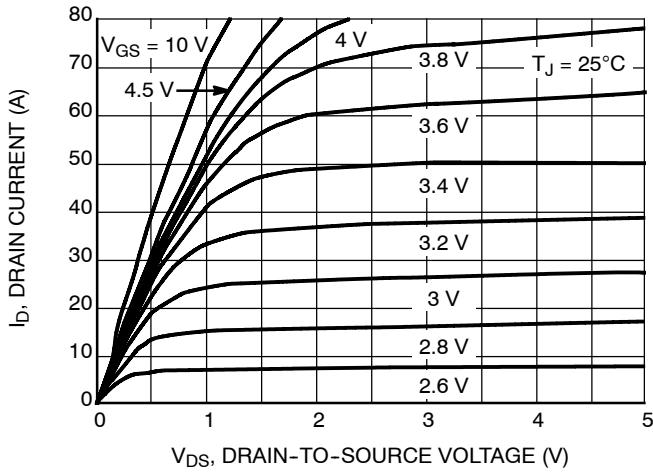


Figure 1. On-Region Characteristics

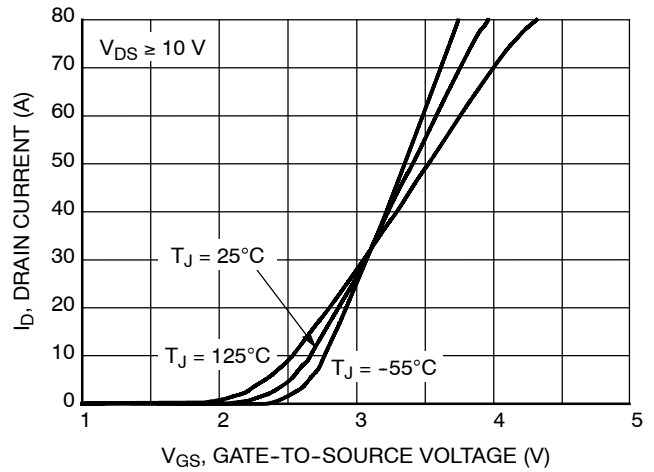


Figure 2. Transfer Characteristics

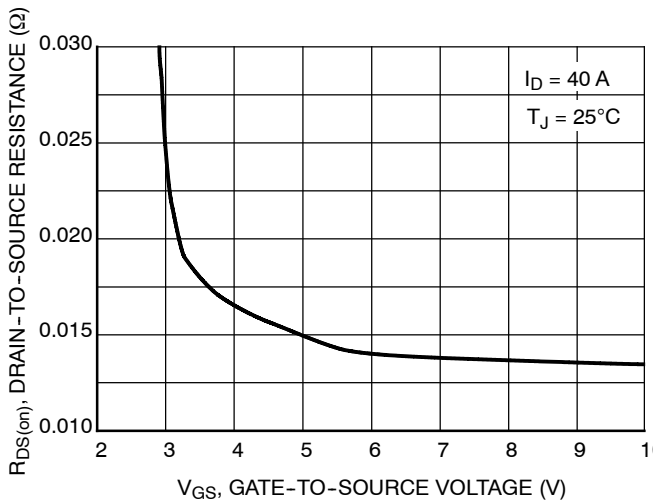


Figure 3. On-Resistance vs. Gate Voltage

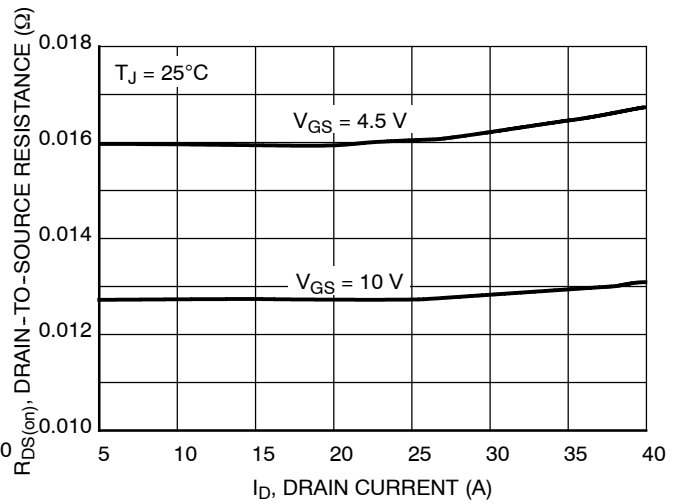


Figure 4. On-Resistance vs. Drain Current

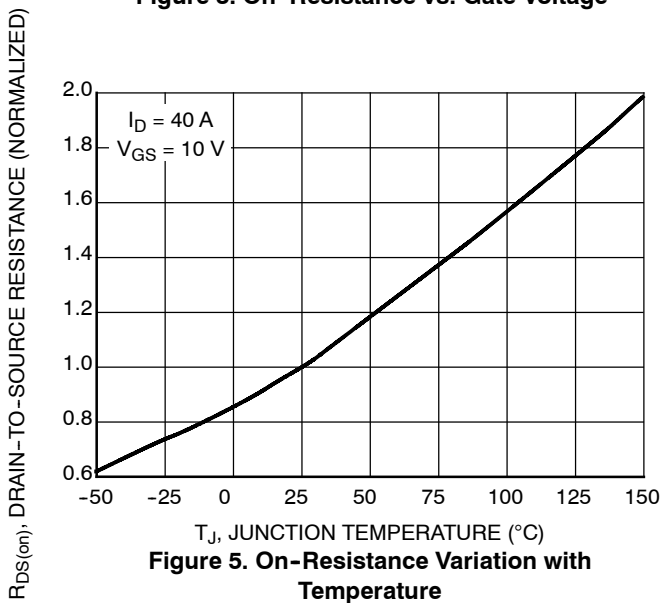


Figure 5. On-Resistance Variation with Temperature

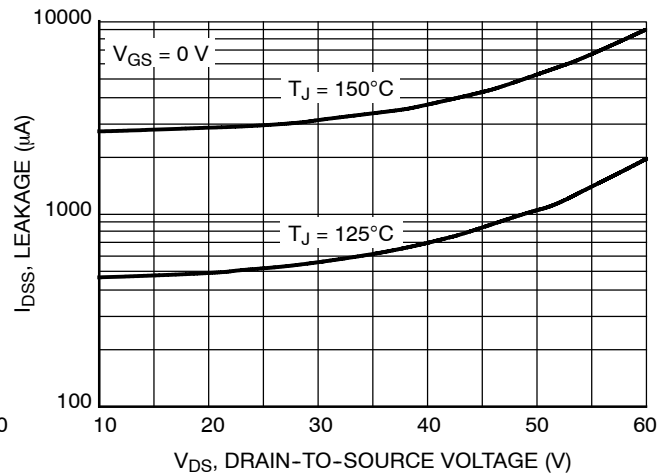


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

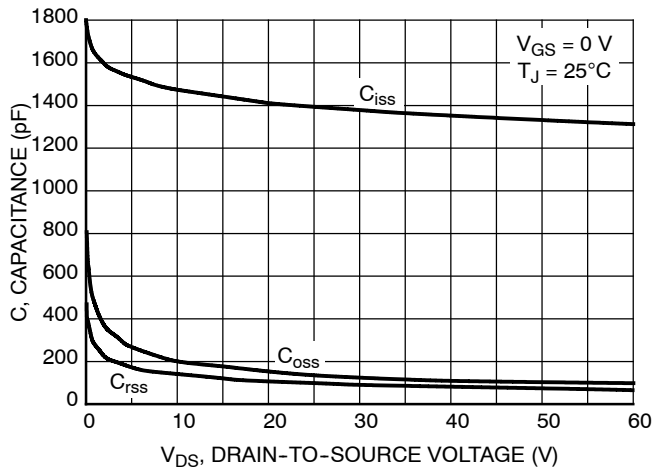


Figure 7. Capacitance Variation

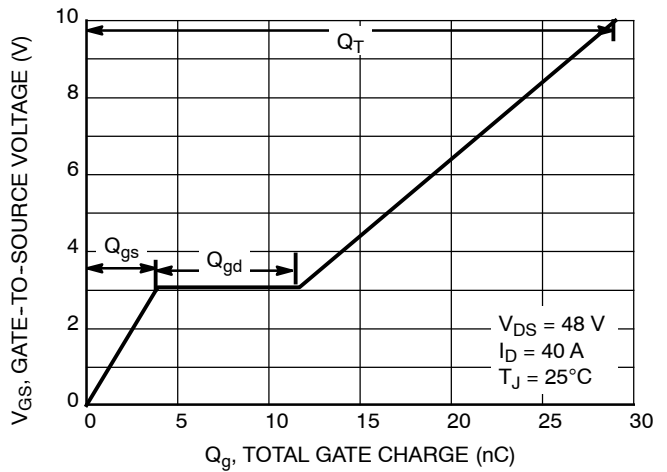


Figure 8. Gate-to-Source vs. Total Charge

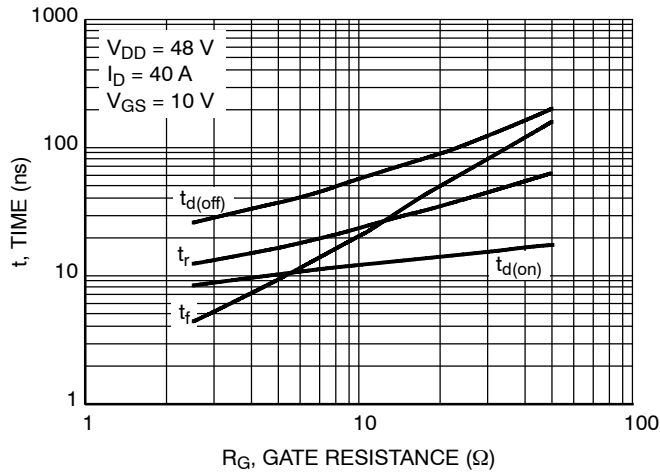


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

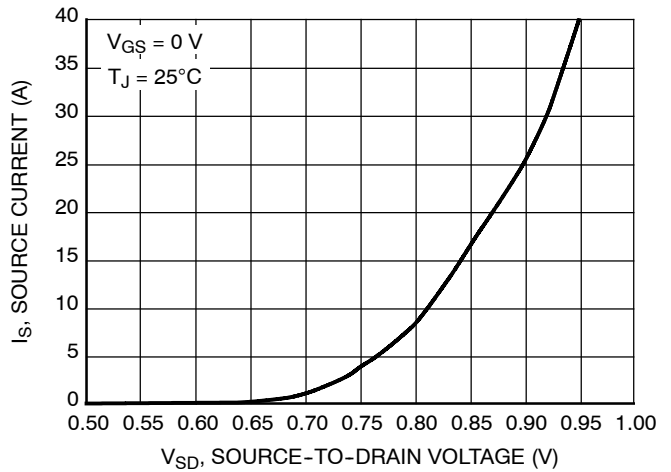


Figure 10. Diode Forward Voltage vs. Current

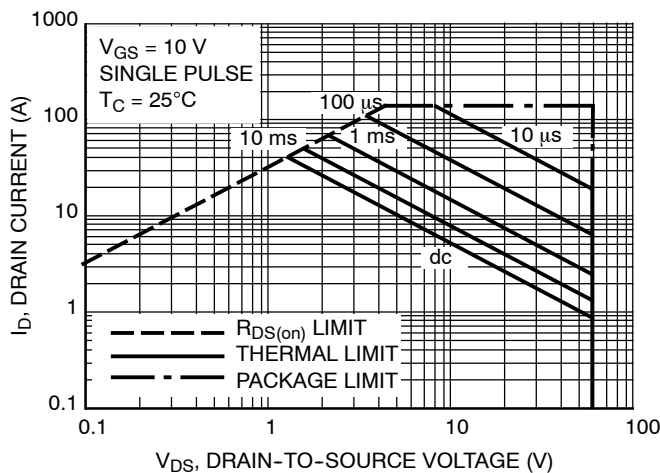


Figure 11. Maximum Rated Forward Biased Safe Operating Area

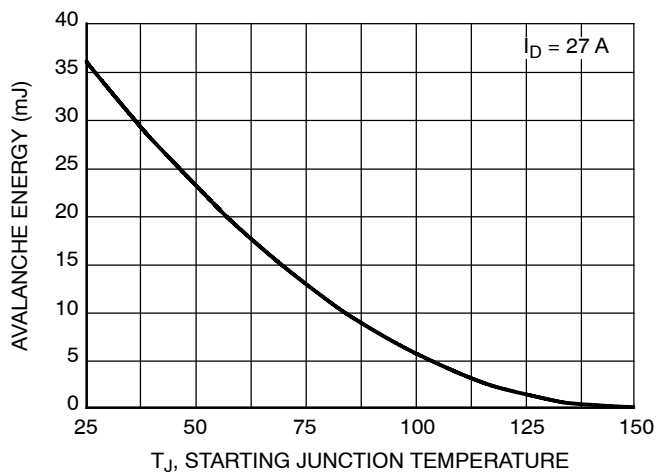


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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TYPICAL CHARACTERISTICS

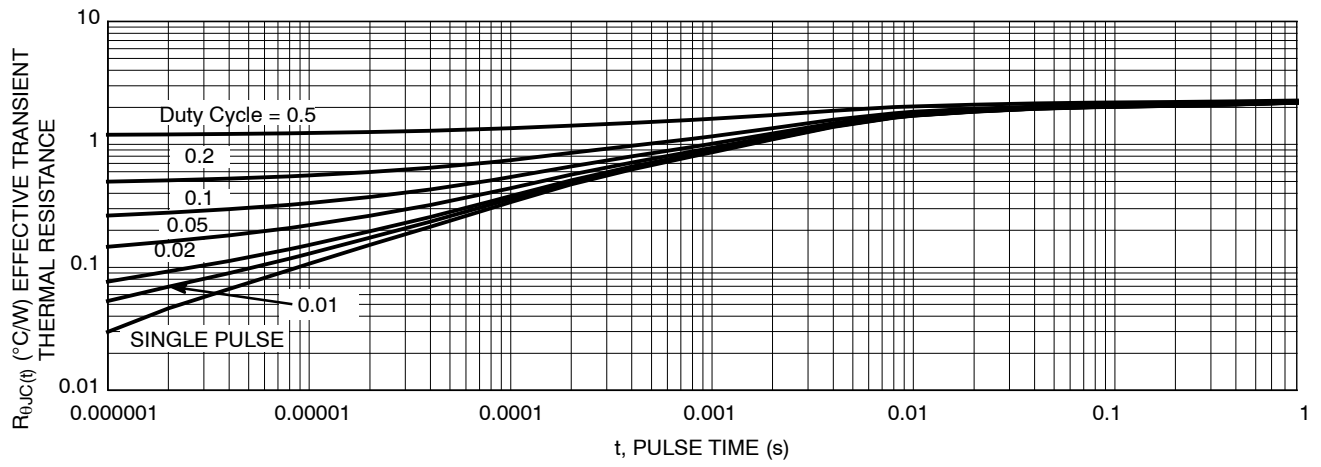
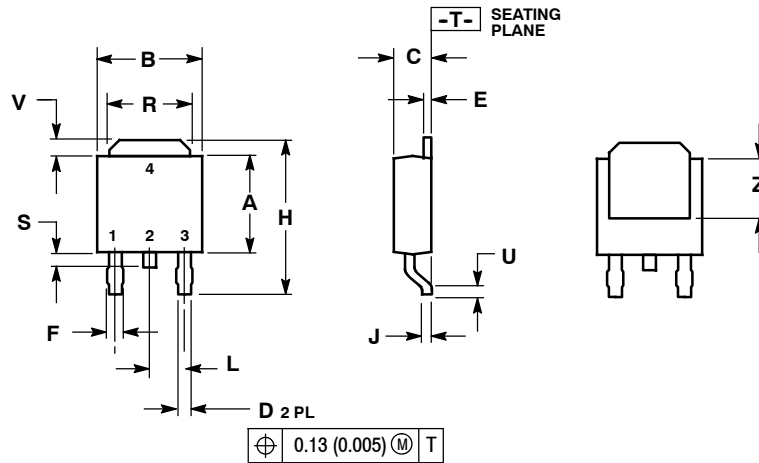


Figure 13. Thermal Response

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PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE) CASE 369AA-01 ISSUE A

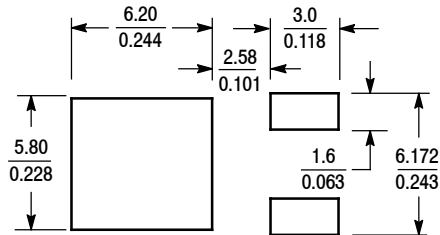


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



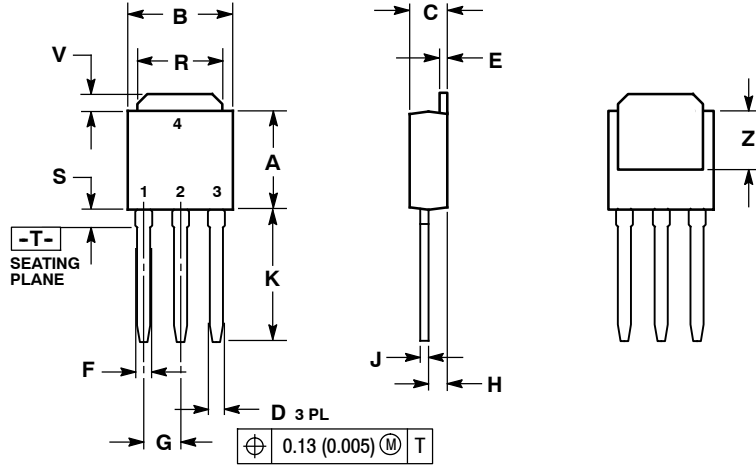
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}} \right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

IPAK CASE 369D-01 ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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