Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics

DS923 (v1.5) February 07, 2018 **Preliminary Product Specification**

Summary

The Xilinx® Virtex® UltraScale+™ FPGAs are available in -3, -2, -1 speed grades, with -3E devices having the highest performance. The -2LE devices can operate at a V_{CCINT} voltage at 0.85V or 0.72V and provide lower maximum static power. When operated at V_{CCINT} = 0.85V, using -2LE devices, the speed specification for the L devices is the same as the -2I speed grade. When operated at V_{CCINT} = 0.72V, the -2LE performance and static and dynamic power is reduced.

DC and AC characteristics are specified in extended (E) and industrial (I) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade extended device are the same as for a -1 speed grade industrial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the Virtex UltraScale+ FPGAs, is available on the Xilinx website at www.xilinx.com/documentation.

DC Characteristics

Absolute Maximum Ratings

Table 1: **Absolute Maximum Ratings**

Symbol	Description[1]	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage	–0.500	1.000	V
V_{CCINT_IO}[2]	Internal supply voltage for the I/O banks	–0.500	1.000	V
V_{CCAUX}	Auxiliary supply voltage	–0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories	–0.500	1.000	V
V_{CCO}	Output drivers supply voltage for HP I/O banks	–0.500	2.000	V
V_{CCAUX_IO}[3]	Auxiliary supply voltage for the I/O banks	–0.500	2.000	V

Table 1: **Absolute Maximum Ratings** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
V_{REF}	Input reference voltage	–0.500	2.000	V
V_{IN}[4, 5, 6]	I/O input voltage for HP I/O banks	–0.550	V_{CCO} + 0.550	V
V_{BATT}	Key memory battery backup supply	–0.500	2.000	V
I_{DC}	Available output current at the pad	–20	20	mA
I_{RMS}	Available RMS output current at the pad	–20	20	mA
GTY Transceiver[7]				
$V_{MGTAVCC}$	Analog supply voltage for transceiver circuits	–0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for transceiver termination circuits	–0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers	–0.500	1.900	V
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage	–0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the transceiver column	–0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	–0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating[8]	–	10	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND[9]	–	0	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable[10]	–	0	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	6	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	6	mA
System Monitor				
V_{CCADC}	System Monitor supply relative to GNDADC	–0.500	2.000	V
V_{REFP}	System Monitor reference input relative to GNDADC	–0.500	2.000	V
Temperature[11]				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum dry rework soldering temperature	–	260	°C
	Maximum reflow soldering temperature	–	245	°C
	Maximum reflow soldering temperature for lidless packages with stiffener ring	–	240	°C

Table 1: **Absolute Maximum Ratings** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
T_j	Maximum junction temperature	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCINT_IO} must be connected to V_{CCBRAM}.
3. V_{CCAUX_IO} must be connected to V_{CCAUX}.
4. The lower absolute voltage specification always applies.
5. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571)
6. When operating outside of the recommended operating conditions, refer to Table 4 for maximum overshoot and undershoot specifications.
7. For more information on supported GTY transceiver terminations see the *UltraScale Architecture GTY Transceivers User Guide* (UG578).
8. AC coupled operation is not supported for RX termination = floating.
9. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
10. DC coupled operation is not supported for RX termination = programmable.
11. For soldering guidelines and thermal considerations, see the *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification* (UG575).

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions**

Symbol	Description[1, 2]	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage	0.825	0.850	0.876	V
	For -2LE (V_{CCINT} = 0.72V) devices: internal supply voltage	0.698	0.720	0.742	V
	For -3E devices: internal supply voltage	0.873	0.900	0.927	V
V_{CCINT_IO}[3]	Internal supply voltage for the I/O banks	0.825	0.850	0.876	V
	For -2LE (V_{CCINT} = 0.72V) devices: internal supply voltage for the I/O banks	0.825	0.850	0.876	V
	For -3E devices: internal supply voltage for the I/O banks	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage	1.746	1.800	1.854	V
V_{CCO}[4, 5]	Supply voltage for I/O banks	0.950	–	1.900	V
V_{CCAUX_IO}[6]	Auxiliary I/O supply voltage	1.746	1.800	1.854	V
V_{IN}[7]	I/O input voltage	–0.200	–	V_{CCO} + 0.200	V
I_{IN}[8]	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA
V_{BATT}[9]	Battery voltage	1.000	–	1.890	V
GTY Transceiver					
$V_{MGTAVCC}$[10]	Analog supply voltage for the GTY transceiver	0.873	0.900	0.927	V
$V_{MGTAVTT}$[10]	Analog supply voltage for the GTY transmitter and receiver termination circuits	1.164	1.200	1.236	V
$V_{MGTVCCAUX}$[10]	Auxiliary analog QPLL voltage supply for the transceivers	1.746	1.800	1.854	V

Table 2: **Recommended Operating Conditions** *(cont'd)*

Symbol	Description[1, 2]	Min	Typ	Max	Units
$V_{MGTAVTTRCAL}$[10]	Analog supply voltage for the resistor calibration circuit of the GTY transceiver column	1.164	1.200	1.236	V
System Monitor					
V_{CCADC}	System Monitor supply relative to GNDADC	1.746	1.800	1.854	V
V_{REFP}	System Monitor externally supplied reference voltage relative to GNDADC	1.200	1.250	1.300	V
Temperature					
T_j[11]	Junction temperature operating range for extended (E) temperature devices[12]	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C
	Junction temperature operating range for eFUSE programming[13]	–40	–	125	°C

Notes:

1. All voltages are relative to GND.
2. For the design of the power distribution system consult the *UltraScale Architecture PCB Design User Guide* (UG583).
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. For V_{CCO_0}, the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if V_{CCO} drops to 0V.
5. Includes V_{CCO} of 1.0V, 1.2V, 1.35V, 1.5V, and1.8V.
6. V_{CCAUX_IO} must be connected to V_{CCAUX}.
7. The lower absolute voltage specification always applies.
8. A total of 200 mA per bank should not be exceeded.
9. If battery is not used, connect V_{BATT} to either GND or V_{CCAUX}.
10. Each voltage listed requires filtering as described in the *UltraScale Architecture GTY Transceivers User Guide* (UG578).
11. Xilinx recommends measuring the T_j of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The system monitor temperature measurement errors (that are described in Table 58) must be accounted for in your design. For example, when using the system monitor with an external reference of 1.25V, and when the system monitor reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted T_j (100°C – 3°C = 97°C).
12. Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature between 100°C and 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation up to T_j = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.
13. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

DC Characteristics Over Recommended Operating Conditions

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.68	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)[2]	–	–	15	µA
C_{IN}[3]	Die input capacitance at the pad	–	–	3.1	pF

Table 3: **DC Characteristics Over Recommended Operating Conditions** *(cont'd)*

Symbol	Description	Min	Typ[1]	Max	Units
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V	60	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V	30	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V	10	–	100	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 1.8V	29	–	120	µA
$I_{CCADCON}$	Analog supply current for the SYSMON circuits in the power-up state	–	–	8	mA
$I_{CCADCOFF}$	Analog supply current for the SYSMON circuits in the power-down state	–	–	1.5	mA
I_{BATT}[4, 5]	Battery supply current at V_{BATT} = 1.89V	–	–	650	nA
	Battery supply current at V_{BATT} = 1.20V	–	–	150	nA
I_{PFS}[6]	V_{CCAUX} additional supply current during eFUSE programming	–	–	115	mA
Calibrated programmable on-die termination (DCI) in I/O banks[7] (measured per JEDEC specification)					
R[9]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40	–10%[8]	40	+10%[8]	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48	–10%[8]	48	+10%[8]	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60	–10%[8]	60	+10%[8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	–10%[8]	40	+10%[8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	–10%[8]	48	+10%[8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	–10%[8]	60	+10%[8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	–10%[8]	120	+10%[8]	Ω
	Programmable input termination to $V_{CCO}$where ODT = RTT_240	–10%[8]	240	+10%[8]	Ω
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					
R[9]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240	–50%	240	+50%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks	–35%	100	+35%	Ω
n	Temperature diode ideality factor	–	1.026	–	–

Table 3: **DC Characteristics Over Recommended Operating Conditions** *(cont'd)*

Symbol	Description	Min	Typ[1]	Max	Units
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For the I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{BATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
7. VRP resistor tolerance is (240Ω ±1%)
8. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
9. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks**

AC Voltage Overshoot[1]	% of UI[2] at –40°C to 100°C	AC Voltage Undershoot[1]	% of UI[2] at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	100%
V_{CCO} + 0.40	92%	–0.40	92%
V_{CCO} + 0.45	50%	–0.45	50%
V_{CCO} + 0.50	20%	–0.50	20%
V_{CCO} + 0.55	10%	–0.55	10%
V_{CCO} + 0.60	6%	–0.60	6%
V_{CCO} + 0.65	2%	–0.65	2%
V_{CCO} + 0.70	2%	–0.70	2%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Quiescent Supply Current

Table 5: **Typical Quiescent Supply Current**

Symbol	Description[1, 2, 3]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XCVU3P	2384	2276	2276	2017	mA
		XCVU5P	4769	4552	4552	4034	mA
		XCVU7P	4769	4552	4552	4034	mA
		XCVU9P	7153	6828	6828	6050	mA
		XCVU11P	7567	7202	7202	6332	mA
		XCVU13P	10090	9602	9602	8442	mA
I_{CCINT_IOQ}	Quiescent V_{CCINT_IO} supply current	XCVU3P	149	144	144	144	mA
		XCVU5P	298	287	287	287	mA
		XCVU7P	298	287	287	287	mA
		XCVU9P	447	431	431	431	mA
		XCVU11P	182	176	176	176	mA
		XCVU13P	243	234	234	234	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	All devices	1	1	1	1	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XCVU3P	268	268	268	268	mA
		XCVU5P	535	535	535	535	mA
		XCVU7P	535	535	535	535	mA
		XCVU9P	1015	1015	1015	1015	mA
		XCVU11P	819	819	819	819	mA
		XCVU13P	1091	1091	1091	1091	mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XCVU3P	62	62	62	62	mA
		XCVU5P	124	124	124	124	mA
		XCVU7P	124	124	124	124	mA
		XCVU9P	187	187	187	187	mA
		XCVU11P	79	79	79	79	mA
		XCVU13P	105	105	105	105	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XCVU3P	45	43	43	43	mA
		XCVU5P	90	85	85	85	mA
		XCVU7P	90	85	85	85	mA
		XCVU9P	134	128	128	128	mA
		XCVU11P	130	124	124	124	mA
		XCVU13P	174	165	165	165	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions or supplies other than those specified.

Power Supply Sequencing

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTY transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCQ} maximum, required by each Virtex UltraScale+ FPGA for proper power-on and configuration. If these current minimums are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies. The XPE spreadsheet tool (download at http://www.xilinx.com/power) is also used to estimate power-on current for all supplies.

Table 6: **Power-on Current by Device**

Device	$I_{CCINTMIN}$	$I_{CCINT\_IOMIN} + I_{CCBRAMMIN}$	I_{CCOMIN}	$I_{CCAUXMIN} + I_{CCAUX\_IOMIN}$	Units
XCVU3P	I_{CCINTQ} + 2000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 950	I_{CCOQ} + 50	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 350	mA
XCVU5P	I_{CCINTQ} + 4000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 1900	I_{CCOQ} + 100	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 700	mA
XCVU7P	I_{CCINTQ} + 4000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 1900	I_{CCOQ} + 100	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 700	mA
XCVU9P	I_{CCINTQ} + 6000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 2850	I_{CCOQ} + 150	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1050	mA
XCVU11P	I_{CCINTQ} + 6549	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 3111	I_{CCOQ} + 164	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1146	mA
XCVU13P	I_{CCINTQ} + 8731	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 4148	I_{CCOQ} + 219	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1528	mA

Table 7: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO}	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

I/O Levels

Table 8: **SelectIO DC Input and Output Levels for I/O Banks**

I/O Standard[1, 2, 3]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470	7.0	–7.0
MIPI_DPHY_ DCI_LP[6]	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 9, Table 13, and Table 14.
4. Supported drive strengths of 2, 4, 6, or 8 mA in I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 9: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards**

I/O Standard[1, 2]	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 10: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]			V_{ILHS}[3]	V_{IHHS}[3]	V_{OCM} (V)[4]			V_{OD} (V)[5]		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_DCI_HS[7]	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. LVDS is specified in Table 15.
7. High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 11: **Complementary Differential SelectIO DC Input and Output Levels for I/O Banks**

I/O Standard[1]	V_{ICM} (V)[2]			V_{ID} (V)[3]		V_{OL} (V)[4]	V_{OH} (V)[5]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	–5.8
DIFF_HSTL_I_12	$0.400 \times V_{CCO}$	$V_{CCO}/2$	$0.600 \times V_{CCO}$	0.100	–	$0.250 \times V_{CCO}$	$0.750 \times V_{CCO}$	4.1	–4.1
DIFF_HSTL_I_18	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	0.400	$V_{CCO} - 0.400$	6.2	–6.2
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	$20\% V_{CCO}$	$80\% V_{CCO}$	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0
DIFF_SSTL18_I	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 12, Table 13, Table 14.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 12: **DC Input Levels for Differential POD10 and POD12 I/O Standards**

I/O Standard[1, 2]	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 13: **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards**

Symbol	Description[1, 2]	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance	V_{OM_DC} (as described in Table 14)	36	40	44	Ω
R_{OH}	Pull-up resistance	V_{OM_DC} (as described in Table 14)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 14: **Definitions for DC Output Levels for Single-ended and Differential POD10 and POD12 Standards**

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity)	0.8 x V_{CCO}	V

LVDS DC Specifications (LVDS)

Table 15: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}[1]	Supply voltage		1.710	1.800	1.890	V
V_{ODIFF}[2]	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}[2]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}[3]	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600[3]	mV
V_{ICM_DC}[4]	Input common-mode voltage (DC coupling)		0.300	1.200	1.425	V
V_{ICM_AC}[5]	Input common-mode voltage (AC coupling)		0.600	–	1.100	V

Notes:

1. In I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the Recommended Operating Condition (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in the following table.

Table 16: **Speed Specification Version By Device**

2017.4.1	Device
1.18	XCVU3P, XCVU7P, XCVU9P, XCVU5P, XCVU11P, XCVU13P

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

- **Advance Product Specification:** These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.
- **Preliminary Product Specification:** These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.
- **Product Specification:** These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex UltraScale+ FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 17 correlates the current status of the Virtex UltraScale+ FPGA on a per speed grade basis.

Table 17: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCVU3P	-3E (V_{CCINT} = 0.90V)		-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.72V)[1]
XCVU5P	-3E (V_{CCINT} = 0.90V)		-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.72V)[1]
XCVU7P	-3E (V_{CCINT} = 0.90V)		-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.72V)[1]
XCVU9P	-3E (V_{CCINT} = 0.90V)		-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.72V)[1]

Table 17: **Speed Grade Designations by Device** *(cont'd)*

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCVU11P			-3E (V_{CCINT} = 0.90V) -2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.72V)[1]
XCVU13P			-3E (V_{CCINT} = 0.90V) -2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.72V)[1]

Notes:
1. The lowest power -2L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -2LV.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 18 lists the production released Virtex UltraScale+ FPGA, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 18: **Virtex UltraScale+ FPGA Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages[1]				
	0.90V	0.85V			0.72V
	-3	-2	-1	-2L	-2L
XCVU3P		Vivado tools 2017.1 v1.10		Vivado tools 2017.3.1 v1.16	
XCVU5P		Vivado tools 2017.2 v1.12		Vivado tools 2017.3.1 v1.16	
XCVU7P		Vivado tools 2017.2 v1.12		Vivado tools 2017.3.1 v1.16	
XCVU9P		Vivado tools 2017.2 v1.12		Vivado tools 2017.3.1 v1.16	
XCVU11P	Vivado tools 2017.4.1 v1.18	Vivado tools 2017.2.1 v1.13		Vivado tools 2017.3.1 v1.16	
XCVU13P	Vivado tools 2017.4.1 v1.18	Vivado tools 2017.2.1 v1.13		Vivado tools 2017.3.1 v1.16	

Notes:
1. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the Virtex UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics section.

Table 19: **LVDS Component Mode Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages								Units
	0.90V		0.85V				0.72V		
	-3		-2		-1		-2		
	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)[1]	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)[1]	0	625	0	625	0	625	0	625	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 20: **LVDS Native Mode Performance**

Description[1, 2]	DATA_WIDTH	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.90V		0.85V				0.72V		
		-3		-2		-1		-2		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s
LVDS RX DDR (RX_BITSLICE)[3]	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS RX SDR (RX_BITSLICE)[3]	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_F_{VCOMIN}/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 21: **MIPI D-PHY Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	
MIPI D-PHY transmitter or receiver	1500	1500	1260	1260	Mb/s

Table 22: **LVDS Native-Mode 1000BASE-X Support**

Description[1]	Speed Grade and V_{CCINT} Operating Voltages			
	0.90V	0.85V		0.72V
	-3	-2	-1	-2
1000BASE-X	Yes			

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

The following table provides the maximum data rates for applicable memory standards using the Virtex UltraScale+ FPGA memory PHY. Refer to Memory Interfaces for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design User Guide* (UG583), electrical analysis, and characterization of the system.

Table 23: **Maximum Physical Interface (PHY) Rate for Memory Interfaces**

Memory Standard	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
DDR4	Single rank component	2666	2666	2400	2400	Mb/s
	1 rank DIMM[1, 2, 3]	2400	2400	2133	2133	Mb/s
	2 rank DIMM[1, 4]	2133	2133	1866	1866	Mb/s
	4 rank DIMM[1, 5]	1600	1600	1333	1333	Mb/s
DDR3	Single rank component	2133	2133	2133	2133	Mb/s
	1 rank DIMM[1, 2]	1866	1866	1866	1866	Mb/s
	2 rank DIMM[1, 4]	1600	1600	1600	1600	Mb/s
	4 rank DIMM[1, 5]	1066	1066	1066	1066	Mb/s
DDR3L	Single rank component	1866	1866	1866	1866	Mb/s
	1 rank DIMM[1, 2]	1600	1600	1600	1600	Mb/s
	2 rank DIMM[1, 4]	1333	1333	1333	1333	Mb/s
	4 rank DIMM[1, 5]	800	800	800	800	Mb/s
QDR II+	Single rank component[6]	633	633	600	600	MHz
RLDRAM 3	Single rank component	1200	1200	1066	1066	MHz
QDR IV XP	Single rank component	1066	1066	1066	933	MHz

Table 23: **Maximum Physical Interface (PHY) Rate for Memory Interfaces** *(cont'd)*

Memory Standard	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
LPDDR3	Single rank component	1600	1600	1600	1600	Mb/s

Notes:

1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
2. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
3. For the DDR4 DDP components at -3 and -2 (V_{CCINT} = 0.85V) speed grades, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -3 and -2 (V_{CCINT} = 0.85V) speed grades.
4. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
5. Includes: 2 rank 2 slot, 4 rank 1 slot.
6. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

FPGA Logic Switching Characteristics

Table 24, IOB high-performance (HP), summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF\_DELAY\_PAD\_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{OUTBUF\_DELAY\_O\_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{OUTBUF\_DELAY\_TD\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the DCITERMDISABLE pin is used.

IOB High Performance (HP) Switching Characteristics

Table 24: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
DIFF_HSTL_I_12_F	0.288	0.394	0.402	0.394	0.410	0.423	0.443	0.423	0.514	0.553	0.582	0.553	ns
DIFF_HSTL_I_12_M	0.288	0.394	0.402	0.394	0.552	0.552	0.583	0.552	0.632	0.641	0.679	0.641	ns
DIFF_HSTL_I_12_S	0.288	0.394	0.402	0.394	0.752	0.752	0.800	0.752	0.813	0.813	0.868	0.813	ns
DIFF_HSTL_I_18_F	0.259	0.319	0.339	0.319	0.439	0.456	0.474	0.456	0.549	0.576	0.606	0.576	ns
DIFF_HSTL_I_18_M	0.259	0.319	0.339	0.319	0.563	0.570	0.603	0.570	0.636	0.653	0.692	0.653	ns
DIFF_HSTL_I_18_S	0.259	0.319	0.339	0.319	0.782	0.782	0.834	0.782	0.816	0.816	0.871	0.816	ns
DIFF_HSTL_I_DCI_12_F	0.288	0.394	0.402	0.394	0.393	0.406	0.429	0.406	0.502	0.534	0.564	0.534	ns
DIFF_HSTL_I_DCI_12_M	0.288	0.394	0.402	0.394	0.546	0.557	0.587	0.557	0.636	0.653	0.694	0.653	ns

Table 24: **IOB High Performance (HP) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
DIFF_HSTL_I_DCI_12_S	0.288	0.394	0.402	0.394	0.755	0.755	0.806	0.755	0.842	0.842	0.907	0.842	ns
DIFF_HSTL_I_DCI_18_F	0.259	0.323	0.339	0.323	0.422	0.445	0.461	0.445	0.509	0.566	0.595	0.566	ns
DIFF_HSTL_I_DCI_18_M	0.259	0.323	0.339	0.323	0.546	0.555	0.586	0.555	0.626	0.643	0.684	0.643	ns
DIFF_HSTL_I_DCI_18_S	0.259	0.323	0.339	0.323	0.762	0.762	0.818	0.762	0.836	0.836	0.900	0.836	ns
DIFF_HSTL_I_DCI_F	0.335	0.397	0.417	0.397	0.407	0.431	0.445	0.431	0.517	0.555	0.575	0.555	ns
DIFF_HSTL_I_DCI_M	0.335	0.397	0.417	0.397	0.549	0.553	0.583	0.553	0.634	0.644	0.684	0.644	ns
DIFF_HSTL_I_DCI_S	0.335	0.397	0.417	0.397	0.767	0.767	0.823	0.767	0.848	0.848	0.912	0.848	ns
DIFF_HSTL_I_F	0.304	0.404	0.417	0.404	0.409	0.423	0.443	0.423	0.514	0.549	0.581	0.549	ns
DIFF_HSTL_I_M	0.304	0.404	0.417	0.404	0.549	0.555	0.586	0.555	0.624	0.640	0.677	0.640	ns
DIFF_HSTL_I_S	0.304	0.404	0.417	0.404	0.767	0.767	0.818	0.767	0.811	0.811	0.866	0.811	ns
DIFF_HSUL_12_DCI_F	0.320	0.381	0.400	0.381	0.411	0.425	0.443	0.425	0.520	0.558	0.586	0.558	ns
DIFF_HSUL_12_DCI_M	0.320	0.381	0.400	0.381	0.546	0.557	0.587	0.557	0.636	0.653	0.694	0.653	ns
DIFF_HSUL_12_DCI_S	0.320	0.381	0.400	0.381	0.737	0.737	0.787	0.737	0.822	0.822	0.885	0.822	ns
DIFF_HSUL_12_F	0.322	0.394	0.402	0.394	0.394	0.412	0.430	0.412	0.494	0.538	0.566	0.538	ns
DIFF_HSUL_12_M	0.322	0.394	0.402	0.394	0.552	0.552	0.583	0.552	0.632	0.641	0.679	0.641	ns
DIFF_HSUL_12_S	0.322	0.394	0.402	0.394	0.752	0.752	0.800	0.752	0.813	0.813	0.868	0.813	ns
DIFF_POD10_DCI_F	0.289	0.411	0.430	0.411	0.407	0.425	0.444	0.425	0.512	0.555	0.584	0.555	ns
DIFF_POD10_DCI_M	0.289	0.411	0.430	0.411	0.533	0.542	0.571	0.542	0.618	0.640	0.681	0.640	ns
DIFF_POD10_DCI_S	0.289	0.411	0.430	0.411	0.754	0.754	0.815	0.754	0.850	0.850	0.917	0.850	ns
DIFF_POD10_F	0.288	0.411	0.433	0.411	0.425	0.438	0.459	0.438	0.531	0.569	0.601	0.569	ns
DIFF_POD10_M	0.288	0.411	0.433	0.411	0.519	0.538	0.568	0.538	0.589	0.630	0.667	0.630	ns
DIFF_POD10_S	0.288	0.411	0.433	0.411	0.752	0.766	0.821	0.766	0.821	0.836	0.894	0.836	ns
DIFF_POD12_DCI_F	0.320	0.407	0.432	0.407	0.411	0.425	0.443	0.425	0.519	0.558	0.586	0.558	ns
DIFF_POD12_DCI_M	0.320	0.407	0.432	0.407	0.516	0.543	0.572	0.543	0.602	0.638	0.678	0.638	ns
DIFF_POD12_DCI_S	0.320	0.407	0.432	0.407	0.740	0.772	0.822	0.772	0.833	0.862	0.929	0.862	ns
DIFF_POD12_F	0.305	0.409	0.430	0.409	0.438	0.455	0.476	0.455	0.549	0.595	0.626	0.595	ns
DIFF_POD12_M	0.305	0.409	0.430	0.409	0.551	0.551	0.582	0.551	0.632	0.641	0.679	0.641	ns
DIFF_POD12_S	0.305	0.409	0.430	0.409	0.749	0.767	0.817	0.767	0.818	0.832	0.889	0.832	ns
DIFF_SSTL12_DCI_F	0.303	0.381	0.400	0.381	0.411	0.425	0.443	0.425	0.520	0.558	0.586	0.558	ns
DIFF_SSTL12_DCI_M	0.303	0.381	0.400	0.381	0.549	0.557	0.587	0.557	0.643	0.654	0.694	0.654	ns
DIFF_SSTL12_DCI_S	0.303	0.381	0.400	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
DIFF_SSTL12_F	0.288	0.394	0.402	0.394	0.394	0.412	0.430	0.412	0.494	0.538	0.566	0.538	ns
DIFF_SSTL12_M	0.288	0.394	0.402	0.394	0.550	0.553	0.584	0.553	0.630	0.641	0.676	0.641	ns
DIFF_SSTL12_S	0.288	0.394	0.402	0.394	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
DIFF_SSTL135_DCI_F	0.303	0.371	0.402	0.371	0.392	0.411	0.428	0.411	0.494	0.537	0.565	0.537	ns
DIFF_SSTL135_DCI_M	0.303	0.371	0.402	0.371	0.551	0.551	0.582	0.551	0.643	0.645	0.685	0.645	ns
DIFF_SSTL135_DCI_S	0.303	0.371	0.402	0.371	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
DIFF_SSTL135_F	0.289	0.375	0.402	0.375	0.393	0.408	0.428	0.408	0.491	0.528	0.561	0.528	ns

Table 24: **IOB High Performance (HP) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
DIFF_SSTL135_M	0.289	0.375	0.402	0.375	0.548	0.555	0.585	0.555	0.621	0.641	0.679	0.641	ns
DIFF_SSTL135_S	0.289	0.375	0.402	0.375	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
DIFF_SSTL15_DCI_F	0.335	0.397	0.417	0.397	0.394	0.412	0.429	0.412	0.497	0.531	0.563	0.531	ns
DIFF_SSTL15_DCI_M	0.335	0.397	0.417	0.397	0.549	0.553	0.583	0.553	0.632	0.645	0.685	0.645	ns
DIFF_SSTL15_DCI_S	0.335	0.397	0.417	0.397	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
DIFF_SSTL15_F	0.304	0.404	0.417	0.404	0.409	0.424	0.445	0.424	0.513	0.551	0.577	0.551	ns
DIFF_SSTL15_M	0.304	0.404	0.417	0.404	0.547	0.554	0.585	0.554	0.624	0.639	0.677	0.639	ns
DIFF_SSTL15_S	0.304	0.404	0.417	0.404	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
DIFF_SSTL18_I_DCI_F	0.256	0.320	0.336	0.320	0.422	0.445	0.461	0.445	0.540	0.566	0.595	0.566	ns
DIFF_SSTL18_I_DCI_M	0.256	0.320	0.336	0.320	0.552	0.554	0.585	0.554	0.629	0.644	0.683	0.644	ns
DIFF_SSTL18_I_DCI_S	0.256	0.320	0.336	0.320	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
DIFF_SSTL18_I_F	0.256	0.316	0.336	0.316	0.439	0.454	0.476	0.454	0.549	0.578	0.608	0.578	ns
DIFF_SSTL18_I_M	0.256	0.316	0.336	0.316	0.567	0.571	0.603	0.571	0.535	0.652	0.692	0.652	ns
DIFF_SSTL18_I_S	0.256	0.316	0.336	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
HSLVDCI_15_F	0.336	0.393	0.415	0.393	0.407	0.425	0.443	0.425	0.513	0.548	0.579	0.548	ns
HSLVDCI_15_M	0.336	0.393	0.415	0.393	0.548	0.552	0.581	0.552	0.635	0.644	0.684	0.644	ns
HSLVDCI_15_S	0.336	0.393	0.415	0.393	0.748	0.748	0.802	0.748	0.827	0.827	0.890	0.827	ns
HSLVDCI_18_F	0.367	0.424	0.447	0.424	0.424	0.445	0.461	0.445	0.541	0.566	0.595	0.566	ns
HSLVDCI_18_M	0.367	0.424	0.447	0.424	0.563	0.567	0.598	0.567	0.647	0.658	0.699	0.658	ns
HSLVDCI_18_S	0.367	0.424	0.447	0.424	0.761	0.761	0.817	0.761	0.836	0.836	0.900	0.836	ns
HSTL_I_12_F	0.322	0.378	0.399	0.378	0.410	0.423	0.443	0.423	0.514	0.553	0.582	0.553	ns
HSTL_I_12_M	0.322	0.378	0.399	0.378	0.551	0.551	0.582	0.551	0.632	0.642	0.679	0.642	ns
HSTL_I_12_S	0.322	0.378	0.399	0.378	0.750	0.750	0.799	0.750	0.813	0.813	0.868	0.813	ns
HSTL_I_18_F	0.258	0.322	0.339	0.322	0.439	0.456	0.474	0.456	0.549	0.576	0.606	0.576	ns
HSTL_I_18_M	0.258	0.322	0.339	0.322	0.562	0.569	0.602	0.569	0.637	0.653	0.692	0.653	ns
HSTL_I_18_S	0.258	0.322	0.339	0.322	0.781	0.781	0.833	0.781	0.816	0.816	0.871	0.816	ns
HSTL_I_DCI_12_F	0.322	0.378	0.399	0.378	0.393	0.406	0.429	0.406	0.502	0.534	0.564	0.534	ns
HSTL_I_DCI_12_M	0.322	0.378	0.399	0.378	0.551	0.556	0.586	0.556	0.644	0.654	0.694	0.654	ns
HSTL_I_DCI_12_S	0.322	0.378	0.399	0.378	0.754	0.754	0.803	0.754	0.842	0.842	0.907	0.842	ns
HSTL_I_DCI_18_F	0.258	0.321	0.339	0.321	0.422	0.445	0.461	0.445	0.509	0.566	0.595	0.566	ns
HSTL_I_DCI_18_M	0.258	0.321	0.339	0.321	0.551	0.554	0.585	0.554	0.634	0.643	0.684	0.643	ns
HSTL_I_DCI_18_S	0.258	0.321	0.339	0.321	0.761	0.761	0.817	0.761	0.836	0.836	0.900	0.836	ns
HSTL_I_DCI_F	0.288	0.393	0.415	0.393	0.407	0.431	0.445	0.431	0.517	0.555	0.575	0.555	ns
HSTL_I_DCI_M	0.288	0.393	0.415	0.393	0.548	0.552	0.581	0.552	0.635	0.644	0.684	0.644	ns
HSTL_I_DCI_S	0.288	0.393	0.415	0.393	0.766	0.766	0.821	0.766	0.847	0.847	0.912	0.847	ns
HSTL_I_F	0.322	0.378	0.399	0.378	0.409	0.423	0.443	0.423	0.514	0.549	0.581	0.549	ns
HSTL_I_M	0.322	0.378	0.399	0.378	0.548	0.554	0.585	0.554	0.624	0.640	0.677	0.640	ns
HSTL_I_S	0.322	0.378	0.399	0.378	0.766	0.766	0.816	0.766	0.811	0.811	0.866	0.811	ns

Table 24: **IOB High Performance (HP) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
HSUL_12_DCI_F	0.319	0.378	0.399	0.378	0.411	0.425	0.443	0.425	0.520	0.558	0.586	0.558	ns
HSUL_12_DCI_M	0.319	0.378	0.399	0.378	0.551	0.556	0.586	0.556	0.644	0.654	0.694	0.654	ns
HSUL_12_DCI_S	0.319	0.378	0.399	0.378	0.736	0.736	0.784	0.736	0.821	0.821	0.886	0.821	ns
HSUL_12_F	0.305	0.378	0.399	0.378	0.394	0.412	0.430	0.412	0.494	0.538	0.566	0.538	ns
HSUL_12_M	0.305	0.378	0.399	0.378	0.551	0.551	0.582	0.551	0.632	0.642	0.679	0.642	ns
HSUL_12_S	0.305	0.378	0.399	0.378	0.750	0.750	0.799	0.750	0.813	0.813	0.868	0.813	ns
LVCMOS12_F_2	0.443	0.512	0.555	0.512	0.657	0.672	0.692	0.672	0.862	0.898	0.922	0.898	ns
LVCMOS12_F_4	0.443	0.512	0.555	0.512	0.486	0.504	0.521	0.504	0.645	0.664	0.693	0.664	ns
LVCMOS12_F_6	0.443	0.512	0.555	0.512	0.469	0.485	0.507	0.485	0.585	0.634	0.669	0.634	ns
LVCMOS12_F_8	0.443	0.512	0.555	0.512	0.457	0.465	0.489	0.465	0.592	0.611	0.666	0.611	ns
LVCMOS12_M_2	0.443	0.512	0.555	0.512	0.687	0.708	0.727	0.708	0.889	0.916	0.945	0.916	ns
LVCMOS12_M_4	0.443	0.512	0.555	0.512	0.533	0.550	0.573	0.550	0.629	0.664	0.690	0.664	ns
LVCMOS12_M_6	0.443	0.512	0.555	0.512	0.520	0.527	0.554	0.527	0.608	0.622	0.652	0.622	ns
LVCMOS12_M_8	0.443	0.512	0.555	0.512	0.532	0.540	0.571	0.540	0.606	0.614	0.649	0.614	ns
LVCMOS12_S_2	0.443	0.512	0.555	0.512	0.767	0.767	0.803	0.767	0.981	0.990	1.024	0.990	ns
LVCMOS12_S_4	0.443	0.512	0.555	0.512	0.666	0.666	0.704	0.666	0.803	0.803	0.848	0.803	ns
LVCMOS12_S_6	0.443	0.512	0.555	0.512	0.657	0.657	0.695	0.657	0.732	0.732	0.774	0.732	ns
LVCMOS12_S_8	0.443	0.512	0.555	0.512	0.708	0.708	0.761	0.708	0.745	0.745	0.790	0.745	ns
LVCMOS15_F_12	0.368	0.414	0.445	0.414	0.485	0.500	0.522	0.500	0.584	0.647	0.682	0.647	ns
LVCMOS15_F_2	0.368	0.414	0.445	0.414	0.686	0.702	0.722	0.702	0.893	0.919	0.940	0.919	ns
LVCMOS15_F_4	0.368	0.414	0.445	0.414	0.567	0.579	0.601	0.579	0.727	0.755	0.781	0.755	ns
LVCMOS15_F_6	0.368	0.414	0.445	0.414	0.533	0.547	0.569	0.547	0.684	0.711	0.742	0.711	ns
LVCMOS15_F_8	0.368	0.414	0.445	0.414	0.500	0.518	0.538	0.518	0.635	0.686	0.703	0.686	ns
LVCMOS15_M_12	0.368	0.414	0.445	0.414	0.607	0.607	0.644	0.607	0.637	0.637	0.676	0.637	ns
LVCMOS15_M_2	0.368	0.414	0.445	0.414	0.736	0.741	0.770	0.741	0.929	0.938	0.962	0.938	ns
LVCMOS15_M_4	0.368	0.414	0.445	0.414	0.610	0.625	0.651	0.625	0.733	0.754	0.786	0.754	ns
LVCMOS15_M_6	0.368	0.414	0.445	0.414	0.564	0.576	0.604	0.576	0.655	0.674	0.710	0.674	ns
LVCMOS15_M_8	0.368	0.414	0.445	0.414	0.565	0.568	0.601	0.568	0.634	0.639	0.681	0.639	ns
LVCMOS15_S_12	0.368	0.414	0.445	0.414	0.788	0.788	0.855	0.788	0.695	0.695	0.733	0.695	ns
LVCMOS15_S_2	0.368	0.414	0.445	0.414	0.829	0.829	0.864	0.829	1.038	1.039	1.079	1.039	ns
LVCMOS15_S_4	0.368	0.414	0.445	0.414	0.687	0.687	0.725	0.687	0.813	0.813	0.851	0.813	ns
LVCMOS15_S_6	0.368	0.414	0.445	0.414	0.671	0.671	0.710	0.671	0.726	0.726	0.763	0.726	ns
LVCMOS15_S_8	0.368	0.414	0.445	0.414	0.704	0.704	0.755	0.704	0.721	0.721	0.758	0.721	ns
LVCMOS18_F_12	0.352	0.418	0.445	0.418	0.564	0.573	0.601	0.573	0.696	0.731	0.769	0.731	ns
LVCMOS18_F_2	0.352	0.418	0.445	0.418	0.723	0.739	0.760	0.739	0.918	0.945	0.971	0.945	ns
LVCMOS18_F_4	0.352	0.418	0.445	0.418	0.598	0.609	0.630	0.609	0.749	0.778	0.802	0.778	ns
LVCMOS18_F_6	0.352	0.418	0.445	0.418	0.598	0.603	0.633	0.603	0.781	0.781	0.808	0.781	ns
LVCMOS18_F_8	0.352	0.418	0.445	0.418	0.567	0.573	0.600	0.573	0.712	0.733	0.767	0.733	ns

Table 24: **IOB High Performance (HP) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
LVCMOS18_M_12	0.352	0.418	0.445	0.418	0.640	0.640	0.678	0.640	0.670	0.670	0.709	0.670	ns
LVCMOS18_M_2	0.352	0.418	0.445	0.418	0.785	0.798	0.822	0.798	0.986	0.991	1.016	0.991	ns
LVCMOS18_M_4	0.352	0.418	0.445	0.418	0.658	0.664	0.693	0.664	0.786	0.798	0.836	0.798	ns
LVCMOS18_M_6	0.352	0.418	0.445	0.418	0.625	0.629	0.663	0.629	0.727	0.735	0.775	0.735	ns
LVCMOS18_M_8	0.352	0.418	0.445	0.418	0.626	0.626	0.661	0.626	0.705	0.705	0.746	0.705	ns
LVCMOS18_S_12	0.352	0.418	0.445	0.418	0.795	0.795	0.861	0.795	0.683	0.683	0.721	0.683	ns
LVCMOS18_S_2	0.352	0.418	0.445	0.418	0.861	0.862	0.897	0.862	1.061	1.076	1.098	1.076	ns
LVCMOS18_S_4	0.352	0.418	0.445	0.418	0.716	0.716	0.758	0.716	0.829	0.829	0.872	0.829	ns
LVCMOS18_S_6	0.352	0.418	0.445	0.418	0.682	0.682	0.724	0.682	0.724	0.724	0.762	0.724	ns
LVCMOS18_S_8	0.352	0.418	0.445	0.418	0.707	0.707	0.760	0.707	0.709	0.709	0.745	0.709	ns
LVDCI_15_F	0.369	0.425	0.462	0.425	0.407	0.426	0.443	0.426	0.514	0.548	0.581	0.548	ns
LVDCI_15_M	0.369	0.425	0.462	0.425	0.549	0.553	0.582	0.553	0.632	0.645	0.685	0.645	ns
LVDCI_15_S	0.369	0.425	0.462	0.425	0.749	0.749	0.803	0.749	0.821	0.821	0.890	0.821	ns
LVDCI_18_F	0.367	0.414	0.447	0.414	0.422	0.441	0.459	0.441	0.541	0.560	0.589	0.560	ns
LVDCI_18_M	0.367	0.414	0.447	0.414	0.546	0.554	0.585	0.554	0.622	0.644	0.683	0.644	ns
LVDCI_18_S	0.367	0.414	0.447	0.414	0.760	0.760	0.818	0.760	0.837	0.837	0.899	0.837	ns
LVDS	0.508	0.539	0.620	0.539	0.626	0.626	0.662	0.626	960.447	960.447	960.447	960.447	ns
MIPI_DPHY_DCI_HS	0.305	0.386	0.415	0.386	0.489	0.502	0.522	0.502	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.438	8.438	8.792	8.438	0.895	0.914	0.937	0.914	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.336	0.408	0.430	0.408	0.407	0.425	0.444	0.425	0.512	0.555	0.584	0.555	ns
POD10_DCI_M	0.336	0.408	0.430	0.408	0.533	0.542	0.571	0.542	0.618	0.640	0.681	0.640	ns
POD10_DCI_S	0.336	0.408	0.430	0.408	0.724	0.754	0.815	0.754	0.815	0.850	0.917	0.850	ns
POD10_F	0.336	0.407	0.430	0.407	0.425	0.438	0.459	0.438	0.531	0.569	0.601	0.569	ns
POD10_M	0.336	0.407	0.430	0.407	0.519	0.538	0.568	0.538	0.589	0.630	0.667	0.630	ns
POD10_S	0.336	0.407	0.430	0.407	0.752	0.766	0.821	0.766	0.821	0.836	0.894	0.836	ns
POD12_DCI_F	0.336	0.409	0.431	0.409	0.411	0.425	0.443	0.425	0.519	0.558	0.586	0.558	ns
POD12_DCI_M	0.336	0.409	0.431	0.409	0.516	0.543	0.572	0.543	0.602	0.638	0.678	0.638	ns
POD12_DCI_S	0.336	0.409	0.431	0.409	0.740	0.772	0.822	0.772	0.833	0.862	0.929	0.862	ns
POD12_F	0.336	0.409	0.431	0.409	0.438	0.455	0.476	0.455	0.549	0.595	0.626	0.595	ns
POD12_M	0.336	0.409	0.431	0.409	0.551	0.551	0.582	0.551	0.632	0.641	0.679	0.641	ns
POD12_S	0.336	0.409	0.431	0.409	0.749	0.767	0.817	0.767	0.818	0.832	0.889	0.832	ns
SLVS_400_18	0.492	0.539	0.620	0.539	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.331	0.381	0.399	0.381	0.411	0.425	0.443	0.425	0.520	0.558	0.586	0.558	ns
SSTL12_DCI_M	0.331	0.381	0.399	0.381	0.549	0.557	0.587	0.557	0.643	0.654	0.694	0.654	ns
SSTL12_DCI_S	0.331	0.381	0.399	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
SSTL12_F	0.320	0.403	0.403	0.403	0.394	0.412	0.430	0.412	0.494	0.538	0.566	0.538	ns
SSTL12_M	0.320	0.403	0.403	0.403	0.550	0.553	0.584	0.553	0.630	0.641	0.676	0.641	ns
SSTL12_S	0.320	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns

Table 24: **IOB High Performance (HP) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
SSTL135_DCI_F	0.341	0.366	0.399	0.366	0.392	0.411	0.428	0.411	0.494	0.537	0.565	0.537	ns
SSTL135_DCI_M	0.341	0.366	0.399	0.366	0.551	0.551	0.582	0.551	0.643	0.645	0.685	0.645	ns
SSTL135_DCI_S	0.341	0.366	0.399	0.366	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
SSTL135_F	0.321	0.378	0.399	0.378	0.393	0.408	0.428	0.408	0.491	0.528	0.561	0.528	ns
SSTL135_M	0.321	0.378	0.399	0.378	0.548	0.555	0.585	0.555	0.621	0.641	0.679	0.641	ns
SSTL135_S	0.321	0.378	0.399	0.378	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
SSTL15_DCI_F	0.319	0.402	0.417	0.402	0.394	0.412	0.429	0.412	0.497	0.531	0.563	0.531	ns
SSTL15_DCI_M	0.319	0.402	0.417	0.402	0.549	0.553	0.583	0.553	0.632	0.645	0.685	0.645	ns
SSTL15_DCI_S	0.319	0.402	0.417	0.402	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
SSTL15_F	0.320	0.371	0.400	0.371	0.393	0.408	0.428	0.408	0.494	0.530	0.556	0.530	ns
SSTL15_M	0.320	0.371	0.400	0.371	0.547	0.554	0.585	0.554	0.624	0.639	0.677	0.639	ns
SSTL15_S	0.320	0.371	0.400	0.371	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
SSTL18_I_DCI_F	0.256	0.329	0.336	0.329	0.422	0.445	0.461	0.445	0.540	0.566	0.595	0.566	ns
SSTL18_I_DCI_M	0.256	0.329	0.336	0.329	0.552	0.554	0.585	0.554	0.629	0.644	0.683	0.644	ns
SSTL18_I_DCI_S	0.256	0.329	0.336	0.329	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
SSTL18_I_F	0.259	0.316	0.337	0.316	0.439	0.454	0.476	0.454	0.549	0.578	0.608	0.578	ns
SSTL18_I_M	0.259	0.316	0.337	0.316	0.567	0.571	0.603	0.571	0.535	0.652	0.692	0.652	ns
SSTL18_I_S	0.259	0.316	0.337	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
SUB_LVDS	0.508	0.539	0.620	0.539	0.658	0.660	0.692	0.660	907.387	969.863	969.863	969.863	ns

IOB 3-state Output Switching Characteristics

Table 25 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$.

- $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).
- $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output.
- In I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used.

Table 25: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
$T_{OUTBUF\_DELAY\_TE\_PAD}$	T input to pad high-impedance for the I/O banks	5.330	5.330	5.341	5.330	ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for the I/O banks	0.873	0.936	1.037	0.936	ns

Input Delay Measurement Methodology

The following table shows the test setup parameters used for measuring input delay.

Table 26: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L [1, 2]	V_H [1, 2]	V_{MEAS} [1, 4]	V_{REF} [1, 3, 5]
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, LVDCI, HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVCMOS, LVDCI, HSLVDCI, 1.8V	LVCMOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL135, 1.35V	SSTL135	V_{REF} – 0.2875	V_{REF} + 0.2875	V_{REF}	0.675
SSTL15, 1.5V	SSTL15	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
SSTL18, class I, 1.8V	SSTL18_I	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
POD10, 1.0V	POD10	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.7
POD12, 1.2V	POD12	V_{REF} – 0.24	V_{REF} + 0.24	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.25	0.6 + 0.25	0[6]	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	0.75 – 0.325	0.75 + 0.325	0[6]	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	0.9 – 0.4	0.9 + 0.4	0[6]	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.25	0.6 + 0.25	0[6]	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.25	0.6 + 0.25	0[6]	–
DIFF_SSTL135, 1.35V	DIFF_SSTL135	0.675 – 0.2875	0.675 + 0.2875	0[6]	–
DIFF_SSTL15, 1.5V	DIFF_SSTL15	0.75 – 0.325	0.75 + 0.325	0[6]	–
DIFF_SSTL18_I, 1.8V	DIFF_SSTL18_I	0.9 – 0.4	0.9 + 0.4	0[6]	–
DIFF_POD10, 1.0V	DIFF_POD10	0.5 – 0.2	0.5 + 0.2	0[6]	–
DIFF_POD12, 1.2V	DIFF_POD12	0.6 – 0.25	0.6 + 0.25	0[6]	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0[6]	–
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0[6]	–

Table 26: **Input Delay Measurement Methodology** *(cont'd)*

Description	I/O Standard Attribute	V_L [1, 2]	V_H [1, 2]	V_{MEAS} [1, 4]	V_{REF} [1, 3, 5]
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0[6]	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0[6]	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0[6]	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

Figure 1: **Single-Ended Test Setup**

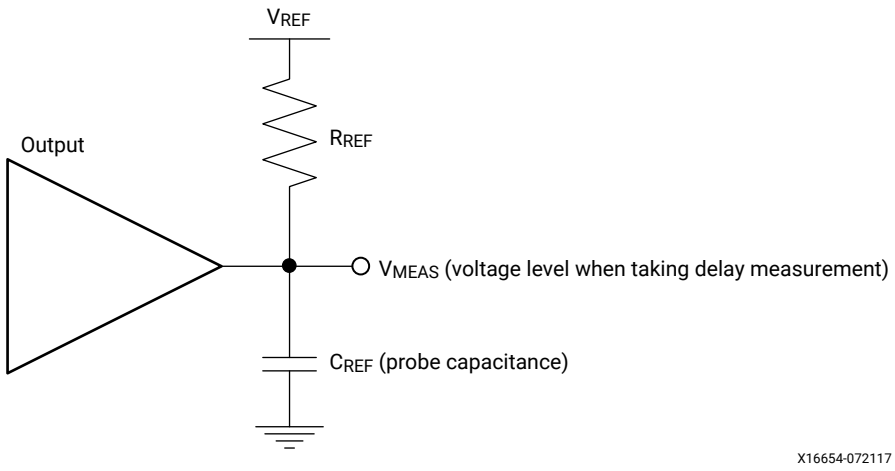
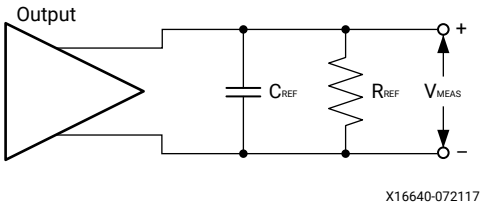


Figure 2: **Differential Test Setup**



Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 27.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 27: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135, 1.35V	SSTL135	50	0	V_{REF}	0.675
SSTL15, 1.5V	SSTL15	50	0	V_{REF}	0.75
SSTL18, class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V_{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V_{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135, 1.35V	DIFF_SSTL135	50	0	V_{REF}	0.675
DIFF_SSTL15, 1.5V	DIFF_SSTL15	50	0	V_{REF}	0.75
DIFF_SSTL18, 1.8V	DIFF_SSTL18_I	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[2]	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0[2]	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0[2]	0

Table 27: **Output Delay Measurement Methodology** *(cont'd)*

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Block RAM and FIFO Switching Characteristics

Table 28: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Maximum Frequency						
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes)	825	737	645	585	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode)	718	637	575	510	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	825	737	645	585	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE	718	637	575	510	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode	825	737	645	585	MHz
T_{PW}[1]	Minimum pulse width	495	542	543	577	ps
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)	0.91	1.02	1.11	1.46	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)	0.27	0.29	0.30	0.42	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

UltraRAM Switching Characteristics

The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists the Virtex UltraScale+ FPGAs that include this memory.

Table 29: **UltraRAM Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Maximum Frequency						
F_{MAX}	UltraRAM maximum frequency with OREG_B = True	650	600	575	500	MHz
$F_{MAX\_ECC\_NOPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = True	435	400	386	312	MHz
$F_{MAX\_NOPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False	528	500	478	404	MHz
T_{PW}[1]	Minimum pulse width	650	700	730	800	ps
T_{RSTPW}	Asynchronous reset minimum pulse width. One cycle required	1 clock cycle				

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Input/Output Delay Switching Characteristics

Table 30: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
F_{REFCLK}	Reference clock frequency for IDELAYCTRL (component mode)	300 to 800				MHz
	Reference clock frequency when using BITSLICE_CONTROL with REFCLK (in native mode (for RX_BITSLICE only))	300 to 800				MHz
	Reference clock frequency for BITSLICE_CONTROL with PLL_CLK (in native mode)[1]	300 to 2666.67	300 to 2666.67	300 to 2400	300 to 2400	MHz
T_{MINPER_CLK}	Minimum period for IODELAY clock	3.195	3.195	3.195	3.195	ns
T_{MINPER_RST}	Minimum reset pulse width	52.00				ns
$T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$	IDELAY/ODELAY chain resolution	2.1 to 12				ps

Notes:

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_F_{VCOMIN}/2.

DSP48 Slice Switching Characteristics

Table 31: **DSP48 Slice Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V[1]	
		-3	-2	-1	-2	
Maximum Frequency						
F_{MAX}	With all registers used	891	775	645	644	MHz
F_{MAX_PATDET}	With pattern detector	794	687	571	562	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	635	544	456	440	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	577	492	410	395	MHz
$F_{MAX\_PREADD\_NOADREG}$	Without ADREG	655	565	468	453	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	483	410	338	323	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	448	379	314	299	MHz

Notes:

1. For devices operating at the lower power V_{CCINT} = 0.72V voltages, DSP cascades that cross clock region boundaries might operate below the specified F_{MAX}.

Clock Buffers and Networks

Table 32: **Clock Buffers Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Global Clock Switching Characteristics (Including BUFGCTRL)						
F_{MAX}	Maximum frequency of a global clock tree (BUFG)	891	775	667	725	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)						
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV)	891	775	667	725	MHz
Global Clock Buffer with Clock Enable (BUFGCE)						
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE)	891	775	667	725	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)						
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF)	891	775	667	725	MHz
GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)						
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability	512	512	512	512	MHz

MMCM Switching Characteristics

Table 33: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
MMCM_F_{INMAX}	Maximum input clock frequency	1066	933	800	933	MHz
MMCM_F_{INMIN}	Minimum input clock frequency	10	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
MMCM_F_{INDUTY}	Input duty cycle range: 10–49 MHz	25–75				%
	Input duty cycle range: 50–199 MHz	30–70				%
	Input duty cycle range: 200–399 MHz	35–65				%
	Input duty cycle range: 400–499 MHz	40–60				%
	Input duty cycle range: >500 MHz	45–55				%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	550	500	450	500	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency	800	800	800	800	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency	1600	1600	1600	1600	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical[1]	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical[1]	4.00	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs[2]	0.12	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter	Note 3				
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision[4]	0.165	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time for MMCM_F_{PFDMIN}	100	100	100	100	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency	891	775	667	725	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency[4, 5]	6.25	6.25	6.25	6.25	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector	550	500	450	500	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector	10	10	10	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path	5 ns Max or one clock cycle				
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

PLL Switching Characteristics

Table 34: **PLL Specification**

Symbol	Description[1]	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
PLL_F_{INMAX}	Maximum input clock frequency	1066	933	800	933	MHz
PLL_F_{INMIN}	Minimum input clock frequency	70	70	70	70	MHz
$PLL\_F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Input duty cycle range: 70–399 MHz	35–65				%
	Input duty cycle range: 400–499 MHz	40–60				%
	Input duty cycle range: >500 MHz	45–55				%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency	750	750	750	750	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency	1500	1500	1500	1500	MHz
$PLL\_T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs[2]	0.12	0.12	0.12	0.12	ns
$PLL\_T_{OUTJITTER}$	PLL output jitter	Note 3				
$PLL\_T_{OUTDUTY}$	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision[4]	0.165	0.20	0.20	0.20	ns
$PLL\_T_{LOCKMAX}$	PLL maximum lock time	100				µs
PLL_F_{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B	891	775	667	725	MHz
	PLL maximum output frequency at CLKOUTPHY	2667	2667	2400	2400	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B[5]	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY	2 x VCO mode: 1500, 1 x VCO mode: 750, 0.5 x VCO mode: 375				MHz
$PLL\_RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	667.5	667.5	667.5	667.5	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	70	70	70	70	MHz
$PLL\_F_{BANDWIDTH}$	PLL bandwidth at typical	14	14	14	14	MHz
$PLL\_F_{DPRCLK\_MAX}$	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 35: **Global Clock Input to Output Delay Without MMCM (Near Clock Region)**

Symbol	Description[1]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM							
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM (near clock region)	XCVU3P	4.41	4.77	5.09	5.48	ns
		XCVU5P	4.41	4.77	5.09	5.48	ns
		XCVU7P	4.41	4.77	5.09	5.48	ns
		XCVU9P	4.41	4.77	5.09	5.48	ns
		XCVU11P	4.22	4.59	4.90	5.27	ns
		XCVU13P	4.22	4.59	4.90	5.27	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 36: **Global Clock Input to Output Delay Without MMCM (Far Clock Region)**

Symbol	Description[1]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM							
T_{ICKOF_FAR}	Global clock input and output flip-flop *without* MMCM (far clock region)	XCVU3P	4.90	5.33	5.69	6.24	ns
		XCVU5P	4.90	5.33	5.69	6.24	ns
		XCVU7P	4.90	5.33	5.69	6.24	ns
		XCVU9P	4.90	5.33	5.69	6.24	ns
		XCVU11P	4.40	4.79	5.11	5.54	ns
		XCVU13P	4.40	4.79	5.11	5.54	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 37: **Global Clock Input to Output Delay With MMCM**

Symbol	Description[1, 2]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM							
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM	XCVU3P	1.51	1.80	1.94	1.80	ns
		XCVU5P	1.51	1.80	1.94	1.80	ns
		XCVU7P	1.51	1.80	1.94	1.80	ns
		XCVU9P	1.51	1.80	1.94	1.80	ns
		XCVU11P	1.29	1.56	1.68	1.56	ns
		XCVU13P	1.29	1.56	1.68	1.56	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in the following table are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 38: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages				Units
				0.90V	0.85V		0.72V	
				-3	-2	-1	-2	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.[1, 2, 3]								
$T_{PSMMCMCC\_VU3P}$	Global clock input and input flip-flop (or latch) with MMCM	Setup	XCVU3P	1.86	1.86	1.99	1.86	ns
$T_{PHMMCMCC\_VU3P}$		Hold		–0.13	–0.13	–0.13	–0.17	ns
$T_{PSMMCMCC\_VU5P}$		Setup	XCVU5P	1.86	1.86	1.99	1.86	ns
$T_{PHMMCMCC\_VU5P}$		Hold		–0.13	–0.13	–0.13	–0.17	ns
$T_{PSMMCMCC\_VU7P}$		Setup	XCVU7P	1.86	1.86	1.99	1.86	ns
$T_{PHMMCMCC\_VU7P}$		Hold		–0.13	–0.13	–0.13	–0.17	ns
$T_{PSMMCMCC\_VU9P}$		Setup	XCVU9P	1.86	1.86	1.99	1.86	ns
$T_{PHMMCMCC\_VU9P}$		Hold		–0.13	–0.13	–0.13	–0.17	ns
$T_{PSMMCMCC\_VU11P}$		Setup	XCVU11P	1.91	1.92	2.05	1.92	ns
$T_{PHMMCMCC\_VU11P}$		Hold		–0.13	–0.13	–0.13	–0.18	ns
$T_{PSMMCMCC\_VU13P}$		Setup	XCVU13P	1.91	1.92	2.05	1.92	ns
$T_{PHMMCMCC\_VU13P}$		Hold		–0.13	–0.13	–0.13	–0.18	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 39: **Sampling Window**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	
T_{SAMP_BUFG}[1]	510	610	610	610	ps
$T_{SAMP\_NATIVE\_DPA}$	100	100	125	125	ps
$T_{SAMP\_NATIVE\_BISC}$	60	60	85	85	ps

Notes:

1. This parameter indicates the total sampling error of the Virtex UltraScale+ FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 40: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew[1, 2]	XCVU3P	FFVC1517	197	ps
		XCVU5P	FLVA2104	175	ps
			FLVB2104	225	ps
			FLVC2104	216	ps
		XCVU7P	FLVA2104	175	ps
			FLVB2104	225	ps
			FLVC2104	216	ps
		XCVU9P	FLGA2104	217	ps
			FLGB2104	275	ps
			FLGC2104	299	ps
			FSGD2104	229	ps
			FLGA2577	149	ps
		XCVU11P	FLGF1924	180	ps
			FLGB2104	216	ps
			FLGC2104	175	ps
			FSGD2104	224	ps
			FLGA2577	154	ps
		XCVU13P	FHGA2104	215	ps
			FHGB2104	259	ps
			FHGC2104	182	ps
			FIGD2104	198	ps
			FLGA2577	140	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists the Virtex UltraScale+ FPGAs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

Table 41 summarizes the DC specifications of the GTY transceivers in Virtex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceivers User Guide* (UG578) for further details.

Table 41: **GTY Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage[1]	Transmitter output swing is set to 11111	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}[2]	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor[3]		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceivers User Guide* (UG578) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Figure 3: **Single-Ended Peak-to-Peak Voltage**

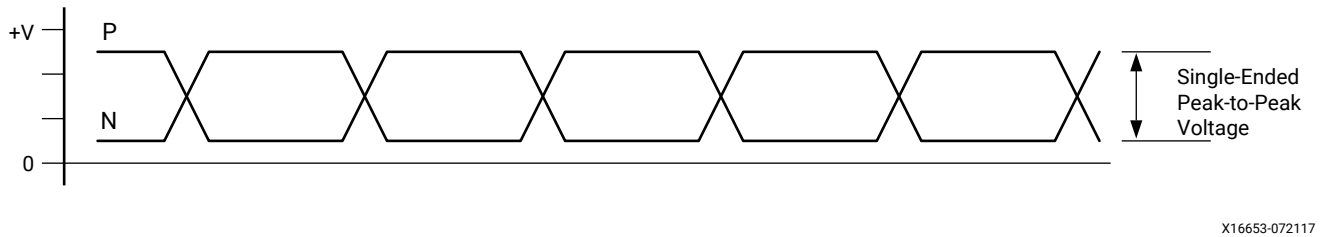
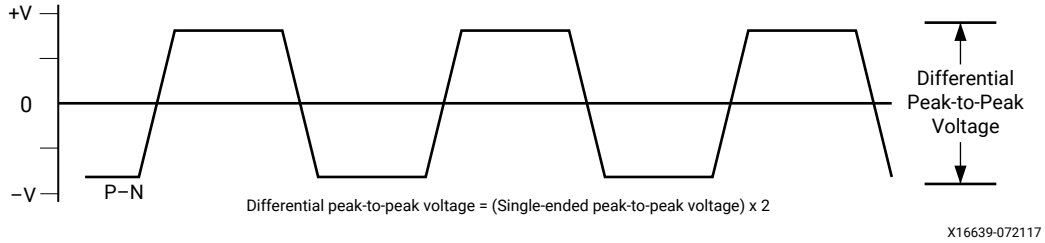


Figure 4: **Differential Peak-to-Peak Voltage**



The following tables summarize the DC specifications of the clock input/output levels of the GTY transceivers in Virtex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceivers User Guide* (UG578) for further details.

Table 42: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 43: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceivers User Guide* (UG578) for further information.

Table 44: **GTY Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages								Units
			0.90V		0.85V				0.72V		
			-3		-2		-1		-2		
F_{GTYMAX}	GTY maximum line rate		32.75[1]		28.21[1]		25.7813[1]		28.21[1]		Gb/s
F_{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYCRANGE}$	CPLL line rate range[2]	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	Gb/s
		16	N/A								Gb/s
		32	N/A								Gb/s

Table 44: **GTY Transceiver Performance** *(cont'd)*

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages								Units
			0.90V		0.85V				0.72V		
			-3		-2		-1		-2		
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE1}$	QPLL0 line rate range[3]	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE2}$	QPLL1 line rate range[4]	1	16.0	26.0	16.0	26.0	16.0	25.7813	16.0	26.0	Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. XCVU11P devices in the FLGF1924 package have a maximum GTY transceiver line rate of 16.3 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 × CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (2 × QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (2 × QPLL1_Frequency)/Output_Divider.

Table 45: **GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency	250	MHz

Table 46: **GTY Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

Table 47: **GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description[1, 2]	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$CPLL_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 48: **GTY Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE)	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled		–	50,000	2.3×10^6	UI

Table 49: **GTY Transceiver User Clock Switching Characteristics**

Symbol	Description[1]	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages				Units
				0.90V	0.85V		0.72V	
		Internal Logic	Interconnect Logic	-3	-2	-1	-2	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.832	402.832	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.832	402.832	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[2] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	MHz
		32	32, 64	511.719	511.719	390.625	390.625	MHz
		64	64, 128	511.719	440.781	402.832	402.832	MHz
		20	20, 40	409.375	409.375	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	MHz
		80	80, 160	409.375	352.625	322.266	352.625	MHz
F_{RXIN}	RXUSRCLK[2] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	MHz
		32	32, 64	511.719	511.719	390.625	390.625	MHz
		64	64, 128	511.719	440.781	402.832	402.832	MHz
		20	20, 40	409.375	409.375	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	MHz
		80	80, 160	409.375	352.625	322.266	352.625	MHz
F_{TXIN2}	TXUSRCLK2[2] maximum frequency	16	16	511.719	511.719	390.625	390.625	MHz
		16	32	255.859	255.859	195.313	195.313	MHz
		32	32	511.719	511.719	390.625	390.625	MHz
		32	64	255.859	255.859	195.313	195.313	MHz
		64	64	511.719	440.781	402.832	402.832	MHz
		64	128	255.859	220.391	201.416	201.416	MHz
		20	20	409.375	409.375	312.500	312.500	MHz
		20	40	204.688	204.688	156.250	156.250	MHz
		40	40	409.375	409.375	312.500	350.000	MHz
		40	80	204.688	204.688	156.250	175.000	MHz
		80	80	409.375	352.625	322.266	352.625	MHz
		80	160	204.688	176.313	161.133	176.313	MHz

Table 49: **GTY Transceiver User Clock Switching Characteristics** *(cont'd)*

Symbol	Description[1]	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages				Units
				0.90V	0.85V		0.72V	
		Internal Logic	Interconnect Logic	-3	-2	-1	-2	
F_{RXIN2}	RXUSRCLK2[2] maximum frequency	16	16	511.719	511.719	390.625	390.625	MHz
		16	32	255.859	255.859	195.313	195.313	MHz
		32	32	511.719	511.719	390.625	390.625	MHz
		32	64	255.859	255.859	195.313	195.313	MHz
		64	64	511.719	440.781	402.832	402.832	MHz
		64	128	255.859	220.391	201.416	201.416	MHz
		20	20	409.375	409.375	312.500	312.500	MHz
		20	40	204.688	204.688	156.250	156.250	MHz
		40	40	409.375	409.375	312.500	350.000	MHz
		40	80	204.688	204.688	156.250	175.000	MHz
		80	80	409.375	352.625	322.266	352.625	MHz
		80	160	204.688	176.313	161.133	176.313	MHz

Notes:

1. Clocking must be implemented as described in the *UltraScale Architecture GTY Transceivers User Guide* (UG578).
2. When the gearbox is used, these maximums refer to the XCLK. For more information, see the Valid Data Width Combinations for TX Asynchronous Gearbox table in the *UltraScale Architecture GTY Transceivers User Guide* (UG578).

Table 50: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew[1]		–	–	500.00	ps
$T_{J32.75}$	Total jitter[2, 4]	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter[2, 4]		–	–	0.19	UI
$T_{J28.21}$	Total jitter[2, 4]	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J16.375}$	Total jitter[2, 4]	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J15.0}$	Total jitter[2, 4]	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter[2, 4]	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter[2, 4]	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J13.1}$	Total jitter[2, 4]	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI

Table 50: **GTY Transceiver Transmitter Switching Characteristics** *(cont'd)*

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J12.5\_QPLL}$	Total jitter[2, 4]	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter[3, 4]	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter[2, 4]	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter[2, 4]	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter[3, 4]	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter[2, 4]	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter[3, 4]	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J8.0}$	Total jitter[3, 4]	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J6.6}$	Total jitter[3, 4]	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J5.0}$	Total jitter[3, 4]	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J4.25}$	Total jitter[3, 4]	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J3.20}$	Total jitter[3, 4]	3.20 Gb/s[5]	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter[3, 4]		–	–	0.10	UI
$T_{J2.5}$	Total jitter[3, 4]	2.5 Gb/s[6]	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter[3, 4]		–	–	0.10	UI
$T_{J1.25}$	Total jitter[3, 4]	1.25 Gb/s[7]	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter[3, 4]		–	–	0.06	UI
T_{J500}	Total jitter[3, 4]	500 Mb/s[8]	–	–	0.10	UI
D_{J500}	Deterministic jitter[3, 4]		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 51: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking[1]	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance[2]						
$J_{T\_SJ32.75}$	Sinusoidal jitter (QPLL)[3]	32.75 Gb/s	0.25	–	–	UI
$J_{T\_SJ28.21}$	Sinusoidal jitter (QPLL)[3]	28.21 Gb/s	0.30	–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)[3]	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL)[3]	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)[3]	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)[3]	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)[3]	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)[3]	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)[3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)[3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL)[3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL)[3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (CPLL)[3]	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (CPLL)[3]	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)[3]	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)[3]	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)[3]	3.2 Gb/s[4]	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)[3]	2.5 Gb/s[5]	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)[3]	1.25 Gb/s[6]	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)[3]	500 Mb/s[7]	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye[2]						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye[8]	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye[8]	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceivers User Guide* (UG578) contains recommended use modes that ensure compliance for the protocols listed in the following table. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 52: **GTY Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant[1]
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant[1]
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR[2]	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI[3]	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI[3]	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant

Table 52: **GTY Transceiver Protocol List** *(cont'd)*

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant[3]
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:
1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale+ Interlaken. The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 53).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 54).
- 12 x 25.78125 Gb/s lane logic only mode (Table 55).

Virtex UltraScale+ FPGAs in the FLVF1924 package are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See the F_{GTYMAX} maximum line rates.

Table 53: **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.90V		0.85V				0.72V		
		-3		-2		-1		-2		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		MHz
		Min[1]	Max	Min[1]	Max	Min[1]	Max	Min[1]	Max	
F_{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:
1. These are the minimum clock frequencies at the maximum lane performance.

Table 54: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.90V		0.85V				0.72V		
		-3[1]		-2[1]		-1		-2		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		MHz
		Min[2]	Max	Min[2]	Max	Min	Max	Min[2]	Max	
F_{CORE_CLK}	Interlaken core clock	412.50[3]	479.20	412.50[3]	479.20	N/A		412.50	429.69	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00[4]	349.52	300.00[4]	349.52	N/A		300.00	349.52	MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT} = 0.85V) and -3 (V_{CCINT} = 0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 55: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	MHz

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale+ Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

Table 56: **Maximum Performance for 100G Ethernet Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2[1]	-1	-2	
F_{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	MHz
F_{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	MHz

Notes:

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

Table 57: **Maximum Performance for PCIE4-based PCI Express Designs**

Symbol	Description[1, 2]	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V[3]	
		-3	-2	-1	-2	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency	500.00	500.00	500.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency	125.00	125.00	125.00	125.00	MHz

Notes:

1. PCI Express Gen4 operation is supported operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.
3. PCI Express Gen3 x16 operation is not supported when V_{CCINT} = 0.72V.

System Monitor Specifications

Table 58: **System Monitor Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy[1]						
Resolution			10	–	–	Bits
Integral nonlinearity[2]	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs

Table 58: **System Monitor Specifications** *(cont'd)*

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral nonlinearity[2]	INL	T_j = –55°C to 125°C	–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic T_j = –55°C to 125°C	–	–	±1	
Analog Inputs[2]						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
On-Chip Sensor Accuracy						
Temperature sensor error[1, 3]		T_j = –55°C to 125°C (with external REF)	–	–	±3	°C
		T_j = –55°C to 110°C (with internal REF)	–	–	±3.5	°C
		T_j = 110°C to 125°C (with internal REF)	–	–	±5	°C
Supply sensor error[4]		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with external REF)	–	–	±0.5	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –40°C to 100°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –55°C to 125°C (with external REF)	–	–	±2.0	%
		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with internal REF)	–	–	±1.0	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with internal REF)	–	–	±2.0	%
		All other supply voltages, T_j = –40°C to 100°C (with internal REF)	–	–	±1.5	%
		All other supply voltages, T_j = –55°C to 125°C (with internal REF)	–	–	±2.5	%
Conversion Rate[5]						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%

Table 58: **System Monitor Specifications** *(cont'd)*

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
SYSMON Reference[6]						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, T_j = –55°C to 125°C	1.225	1.25	1.275	V

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the Analog Input section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. When reading temperature values directly from the PMBus interface, the SYSMON has a +4°C offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of ±3°C becomes +1°C to +7°C when the temperature is read through the PMBus interface.
4. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
5. See the Adjusting the Acquisition Settling Time section in the *UltraScale Architecture System Monitor User Guide* (UG580).
6. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

SYSMON I2C/PMBus Interfaces

Table 59: **SYSMON I2C Fast Mode Interface Switching Characteristics**

Symbol	Description[1]	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	µs
T_{SMFCKH}	SCL High time	0.6	–	µs
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 60: **SYSMON I2C Standard Mode Interface Switching Characteristics**

Symbol	Description[1]	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	µs
T_{SMSCKH}	SCL High time	4.0	–	µs
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Configuration Switching Characteristics

Table 61: **Configuration Switching Characteristics**

Symbol	Description		Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
Power-up Timing Characteristics							
T_{PL}	Program latency		8.5	8.5	8.5	8.5	ms, Max
T_{POR}	Power-on reset (40 ms maximum ramp rate)		65	65	65	65	ms, Max
			0	0	0	0	ms, Min
	Power-on reset with POR override (2 ms maximum ramp rate)		15	15	15	15	ms, Max
			5	5	5	5	ms, Min
$T_{PROGRAM}$	Program pulse width		250	250	250	250	ns, Min
CCLK Output (Master Mode)							
T_{ICCK}	Master CCLK output delay from INIT_B		150	150	150	150	ns, Min
T_{MCCKL}[1]	Master CCLK clock Low time duty cycle		40/60	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle		40/60	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master BPI (x8/x16) SPI (x1/x2/x4) CCLK frequency	XCVU3P, XCVU5P, XCVU7P, XCVU9	125	125	125	100	MHz, Max
	Master SPI (x1/x2/x4) CCLK frequency	XCVU11P, XCVU13P	125	125	125	100	MHz, Max
	Master BPI (x8/x16) SPI (x8) CCLK frequency	XCVU11P, XCVU13P	125	125	125	60	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration		2.7	2.7	2.7	2.7	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK		±15	±15	±15	±15	%, Max
CCLK Input (Slave Mode)							
T_{SCCKL}	Slave CCLK clock minimum Low time		2.5	2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time		2.5	2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave Serial/ Slave SelectMAP CCLK frequency	XCVU3P, XCVU5P, XCVU7P, XCVU9P	125	125	125	100	MHz, Max
	Slave Serial CCLK frequency	XCVU11P, XCVU13P	125	125	125	100	MHz, Max
	Slave SelectMAP CCLK frequency	XCVU11P, XCVU13P	125	125	125	60	MHz, Max
EMCCLK Input (Master Mode)							
T_{EMCCKL}	External master CCLK Low time		2.5	2.5	2.5	2.5	ns, Min
T_{EMCCKH}	External master CCLK High time		2.5	2.5	2.5	2.5	ns, Min
F_{EMCCK}	External master CCLK frequency	XCVU3P, XCVU5P, XCVU7P, XCVU9P	125	125	125	100	MHz, Max
		XCVU11P, XCVU13P	125	125	125	60	MHz, Max

Table 61: **Configuration Switching Characteristics** *(cont'd)*

Symbol	Description		Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
Internal Configuration Access Port							
F_{ICAPCK}	Internal configuration access port (ICAPE3)	XCVU3P	200	200	200	150	MHz, Max
	Master SLR ICAPE3 accessing entire device	XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	125	125	125	125	MHz, Max
	SLR ICAPE3 accessing local SLR	XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	200	200	200	150	MHz, Max
Slave Serial Mode Programming Switching							
T_{DCCK}/T_{CCKD}	D_{IN} setup/hold		3.0/0	3.0/0	3.0/0	4.0/0	ns, Min
T_{CCO}	D_{OUT} clock to out		8.0	8.0	8.0	9.0	ns, Max
SelectMAP Mode Programming Switching							
T_{SMDCCK}/T_{SMCCKD}	D[31:00] setup/hold	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	8.0/0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B setup/hold	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B setup/hold	XCVU3P, XCVU5P, XCVU7P, XCVU9P	10.0/0	10.0/0	10.0/0	11.0/0	ns, Min
		XCVU11P, XCVU13P	11.0/0	11.0/0	11.0/0	17.0/0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required)	XCVU3P, XCVU5P, XCVU7P, XCVU9P	7.0	7.0	7.0	7.0	ns, Max
		XCVU11P, XCVU13P	7.0	7.0	7.0	10.0	ns, Max
T_{SMCO}	D[31:00] clock to out in readback	XCVU3P, XCVU5P, XCVU7P, XCVU9P	8.0	8.0	8.0	8.0	ns, Max
		XCVU11P, XCVU13P	8.0	8.0	8.0	10.0	ns, Max
F_{RBCCK}	Readback frequency	XCVU3P, XCVU5P, XCVU7P, XCVU9P	125	125	125	100	MHz, Max
		XCVU11P, XCVU13P	125	125	125	60	MHz, Max
Boundary-Scan Port Timing Specifications							
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/ hold	XCVU3P	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	8.5/2.0	8.5/2.0	8.5/2.0	8.5/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	XCVU3P	7.0	7.0	7.0	7.0	ns, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	15.0	15.0	15.0	15.0	ns, Max
F_{TCK}	TCK frequency	XCVU3P	66	66	66	66	MHz, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	20	20	20	20	MHz, Max
BPI Master Flash Mode Programming Switching							
T_{BPICCO}	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out		10	10	10	10	ns, Max

Table 61: **Configuration Switching Characteristics** *(cont'd)*

Symbol	Description		Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
T_{BPIDCC}/T_{BPICCD}	D[15:00] setup/hold	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	8.0/0	ns, Min
SPI Master Flash Mode Programming Switching							
T_{SPIDCC}/T_{SPICCD}	D[03:00] setup/hold		3.0/0	3.0/0	3.0/0	4.0/0	ns, Min
T_{SPIDCC}/T_{SPICCD}	D[07:04] setup/hold	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	8.0/0	ns, Min
T_{SPICCM}	MOSI clock to out		8.0	8.0	8.0	8.0	ns, Max
$T_{SPICCM2}$	D[04] clock to out		10.0	10.0	10.0	10.0	ns, Max
$T_{SPICCFC}$	FCS_B clock to out		8.0	8.0	8.0	8.0	ns, Max
$T_{SPICCFC2}$	FCS2_B clock to out		10.0	10.0	10.0	10.0	ns, Max
DNA Port Switching							
F_{DNACK}	DNA port frequency		200	200	200	175	MHz, Max
STARTUPE3 Ports							
$T_{USRCCLKO}$	STARTUPE3 USRCCLKO input port to CCLK pin output delay		0.25/6.00	0.25/6.50	0.25/7.50	0.25/9.00	ns, Min/Max
T_{DO}	DO[3:0] ports to D03-D00 pins output delay		0.25/6.70	0.25/7.70	0.25/8.40	0.25/10.00	ns, Min/Max
T_{DTS}	DTS[3:0] ports to D03-D00 pins 3-state delays		0.25/6.70	0.25/7.70	0.25/8.40	0.25/10.00	ns, Min/Max
T_{FCSBO}	FCSBO port to FCS_B pin output delay		0.25/6.90	0.25/7.50	0.25/8.40	0.25/9.80	ns, Min/Max
T_{FCSBTS}	FCSBTS port to FCS_B pin 3-state delay		0.25/6.90	0.25/7.50	0.25/8.40	0.25/9.80	ns, Min/Max
$T_{USRDONEO}$	USRDONEO port to DONE pin output delay		0.25/8.60	0.25/9.40	0.25/10.50	0.25/12.10	ns, Min/Max
$T_{USRDONETS}$	USRDONETS port to DONE pin 3-state delay		0.25/8.60	0.25/9.40	0.25/10.50	0.25/12.10	ns, Min/Max
T_{DI}	D03-D00 pins to DI[3:0] ports input delay		0.5/2.6	0.5/3.1	0.5/3.5	0.5/4.0	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency		50	50	50	50	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance		±15	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted		4	4	4	4	ms, Max

Notes:

1. When the CCLK is sourced from the EMCCLK pin with a divide-by-one setting, the external EMCCLK must meet this duty-cycle requirement.

Revision History

Date	Version	Description of Revisions
02/07/2018	1.5	Updated Table 16, Table 17, and Table 18 to production release the following devices in Vivado Design Suite 2017.4.1 v1.18. XCVU11P: -3E (V_{CCINT} = 0.90V) XCVU13P: -3E (V_{CCINT} = 0.90V) Revised some of the -3E (V_{CCINT} = 0.90V) speed files in Table 35, Table 36, Table 37, and Table 38. Revised the D_{VPPOUT} control signal in Table 41.
11/28/2017	1.4	In Table 1, corrected the minimum voltage for the section. Updated Table 16, Table 17, and Table 18 to production release all the -2LE (V_{CCINT} = 0.85V) and -2LE (V_{CCINT} = 0.72V) devices/speed/temperature grades in Vivado Design Suite 2017.3.1. Revised the F_{REFCLK} descriptions in Table 30. Revised some of the -3E and -2LE (V_{CCINT} = 0.72V) speed files in Table 35, Table 36, Table 37, Table 38, and added package values to Table 40. Revised the $F_{GTYQRANGE2}$ -1 speed grade minimum in Table 44. Added $T_{SPICCM2}$ and $T_{SPICCFC2}$ to Table 61.
10/02/2017	1.3	Updated Table 1 to include maximum T_{SOL} for dry rework and reflow soldering. Updated Table 16, Table 17, and Table 18 to production release the following devices/speed/temperature grades in Vivado Design Suite 2017.2.1. XCVU11P: -2E, -2I, -1E, -1I XCVU13P: -2E, -2I, -1E, -1I In Table 24, revised the $T_{OUTBUF\_DELAY\_O\_PAD}$ -2 (V_{CCINT} = 0.85V) values for DIFF_SSTL135_S, DIFF_SSTL15_DCI_S, DIFF_SSTL15_S, DIFF_SSTL18_I_DCI_S, and DIFF_SSTL18_I_S. Revised some of the -3E and -2LE (V_{CCINT} = 0.72V) speed files in Table 24, Table 35, Table 36, and Table 37.
06/27/2017	1.2	Updated Table 16, Table 17, and Table 18 to production release the following devices/speed/temperature grades in Vivado Design Suite 2017.2. XCVU5P: -2E, -2I, -1E, -1I XCVU7P: -2E, -2I, -1E, -1I XCVU9P: -2E, -2I, -1E, -1I Updated Note 12 in Table 2 for clarity. In Table 3, removed unsupported voltages (2.5V and 3.3V) from I_{RPU} and I_{RPD}. Added Note 3 to Table 23. Revised the -3E and -2LE (V_{CCINT} = 0.72V) speed files in Table 24, Table 25, Table 35, Table 36, Table 37, and Table 38. In Table 26 removed from the input delay measurement methodology section the following class II I/O standards: SSTL135_II, SSTL15_II, SSTL18_II, DIFF_SSTL135_II, DIFF_SSTL15_II and DIFF_SSTL18_II. Updated the F_{MAX} symbol names and values in Table 29. Added Note 1 to Table 31. Added Note 3 to Table 57. In Table 61, updated the -2LE (V_{CCINT} = 0.72V) specifications for F_{MCCK}, F_{SCCK}, F_{EMCCK}, F_{ICAPCK}, T_{SMDCCK}/T_{SMCCKD}, $T_{SMCKCSO}$, T_{SMCO}, F_{RBCCK}, T_{BPIDCC}/T_{BPICCD}, and T_{SPIDCC}/T_{SPICCD}.
04/19/2017	1.1	Updated the Summary description. In Table 1, updated Note 6, added data, and added Note 7, Note 8, and Note 9. Updated and added data to Table 2 through Table 6. Removed the -1LI speed grade. Updated Table 16, Table 17, and Table 18 to production release in Vivado Design Suite 2017.1 for the XCVU3P: -2E, -2I, -1E, -1I. Updated Table 15. Added Note 1 to Table 17. Updated Table 19, Table 20, Table 24, Table 25, Table 26, Table 28, Table 29, and Table 30. Added Table 21. Added MMCM_F_{DPRCLK_MAX} to Table 33 and PLL_F_{DPRCLK_MAX} to Table 34. Updated to Vivado Design Suite 2017.1 Table 35, Table 36, Table 37, and Table 38. Added data to Table 39 and Table 40. Updated the GTY Transceiver Specifications section. Revised the Integrated Interface Block for Interlaken section. Updated the System Monitor Specifications section adding notes to the tables. Updated the Configuration Switching Characteristics section. Removed the eFUSE Programming Conditions table and added the specifications to Table 2 and Table 3. Updated the Automotive Applications Disclaimer.
04/20/2016	1.0	Initial Xilinx release.

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