

Zynq-7000 All Programmable SoC ZC706 Evaluation Kit (ISE Design Suite 14.5) *Getting Started Guide*

UG961 (v3.0) May 13, 2013



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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/19/12	1.0	Initial Xilinx release.
01/23/13	2.0	<p>Updated for ISE® Design Suite 14.4.</p> <p>Chapter 1: Introduction, page 7 removed "Note: Users of the new Intel® Ivy Bridge . . ." Figure 1-1, the kit photograph, was replaced. In section ZC706 Evaluation Kit Contents, page 8, added this bullet on page 7: "ATX adapter cable, Xilinx part number 2600304." The <i>Key Features</i> section was removed, because features are listed in <i>ZC706 Evaluation Board for the Zynq-7000 XC7Z045 All Programmable SoC User Guide (UG954)</i>.</p> <p>Chapter 2: In Figure 2-2, the switch 4 position changed. In Hardware Test Setup, page 21, the <i>ZC706 Evaluation Kit Contents</i> section was removed.</p> <p>Chapter 3: A note was added on page 22 that though the procedures mention version 14.3, the user should find the latest version of tools online. In Recommended Motherboards, page 22, the boards are now Sandy Bridge and Ivy Bridge. Removed "Tip: The Intel X58 chipsets tend to show higher performance" from page 24. In Figure 3-3, J17 changed to J21. The Figure 3-4 figure title changed to "SW11 SD Boot Mode Settings" and the switch 3 position changed. Added new Figure 3-6 and step 10 above it. The ELF file in step 9, page 25 changed to <code>zynq_pcie_qt.elf</code>, <code>zynq_pcie_cmd.elf</code>. Installing ZC706 Board in the Host Computer Chassis, page 26 now ends with step 8, page 26. Connecting the HDMI cable was added in step 7, page 26. In Host Computer Bootup, page 27, replaced last sentences in step 1. Split step 1 into two steps to show two different actions. Replaced Figure 3-9 and added Table 3-1 to clarify LED settings. LED L and LED R were reversed in step 2 of Host Computer Bootup. Added to step 3, page 29. Replaced Figure 3-15 and Figure 3-16.</p>
05/13/2013	3.0	<p>Replaced all references to <code>zynq_pcie_trd_14_3.zip</code> with <code>zc706-pcie-trd-rdf0287.zip</code> throughout document. Identified location of the PMBus connector in Figure 2-1. Added Note describing SW4 DIP switch setting in ZC706 Evaluation Board Setup, page 10. Removed note on page 22 mentioning ISE Design Suite version 14.3. Updated Figure 3-11, Figure 3-12, and Figure 3-14 screen captures. Revised step 8, page 32. Updated Figure 3-17. Updated links to Xilinx documents and updated link to Zc702 Base TRD (wiki page) http://www.wiki.xilinx.com/Zc702+Base+TRD in Appendix A, Additional Resources.</p>

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Introduction

The ZC706 evaluation kit is based on the Zynq™-7000 XC7Z045 FFG900-2 All Programmable SoC (AP SoC). For additional information, see the product table for the Zynq-7000 family of AP SoCs:

www.xilinx.com/publications/prod_mktg/zynq7000/Zynq-7000-combined-product-table.pdf

A built-in self-test (BIST) and a PCIe® Targeted Reference Design (PCIe TRD) are provided for the ZC706 evaluation kit. The BIST provides a convenient way to test many of the board's features on power-up and upon reconfiguration. The PCIe TRD showcases various features and capabilities of the Zynq-7000 Z-7045 AP SoC for the embedded domain in a single package. The tutorials and reference designs available on the ZC706 web page can be used to further explore the capabilities of the ZC706 board and the Zynq-7000 AP SoC. For the most up-to-date information on the tutorial content provided with the ZC706 evaluation kit, go to the Xilinx Zynq-7000 AP SoC ZC706 Evaluation Kit web page at www.xilinx.com/ZC706 and click on the **Docs & Designs** tab.



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Figure 1-1: Zynq-7000 XC7Z045 FFG900-2 All Programmable SoC Evaluation Kit

ZC706 Evaluation Kit Contents

The ZC706 evaluation kit includes the following items:

- ZC706 evaluation board (EK-Z7-ZC706-CES-G) featuring the XC7Z045 FFG900-2 AP SoC
- Full seat ISE® Design Suite: Embedded Edition
 - Device-locked to the XC7Z045 FFG900-2 AP SoC
- Board design files
 - Schematics
 - Board layout files
 - Bill of Material (BOM)
- Documentation
 - [UG954](#), *ZC706 Evaluation Board for the Zynq-7000 XC7Z045 All Programmable SoC User Guide*
 - [UG961](#), *Zynq-7000 All Programmable SoC ZC706 Evaluation Kit Getting Started Guide* (this document)
 - [UG963](#), *Zynq-7000 All Programmable SoC ZC706 PCI Express Targeted Reference Design User Guide*
- 12V AC adapter power supply
- Cables
 - RJ45 Ethernet cable
 - HDMI cable
 - Digilent USB JTAG Cable
 - USB Type-A to USB Mini-B cable
- Secure Digital (SD) multimedia card
- The Fedora 16.2 LiveDVD
- ATX adapter cable (Xilinx part number 2600304)

The evaluation kit contains all the software and reference designs, demonstrations, and documentation needed to help the user get started quickly.

For reference design files, documents, and board source files, go to the ZC706 Product Page at www.xilinx.com/zc706 and click on the **Docs & Designs** tab.

Refer to *ZC706 Evaluation Board for the Zynq-7000 XC7Z045 All Programmable SoC User Guide* ([UG954](#)) for a list of key features available on ZC706 evaluation kit.

ZC706 Evaluation Kit Built-In Self-Test

Introduction

The built-in self-test (BIST) tests many of the features offered by the Zynq-7000 All Programmable SoC ZC706 evaluation kit. The test is available after programming the FPGA through JTAG.

Figure 2-1 provides an overview of the board features utilized by the BIST.

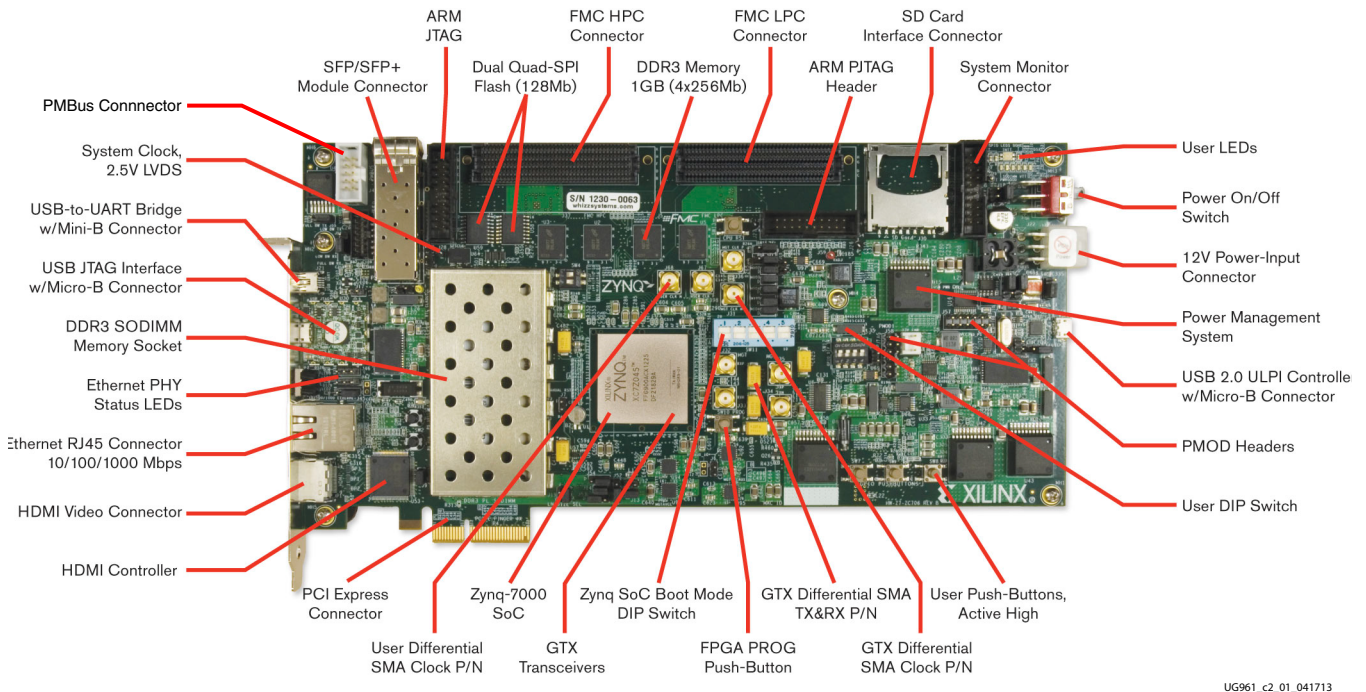


Figure 2-1: ZC706 Board Features

Note: For a diagram of all the features on the ZC706 board, see [UG954](#), ZC706 Evaluation Board for the Zynq-7000 XC7Z045 All Programmable SoC User Guide.

Built-In Self-Test Setup Requirements

The prerequisites for testing the design in hardware are:

- ZC706 evaluation board with the Zynq-7000 XC7Z045 FFG900-2 AP SoC part
- USB to Mini-B cable (for UART)
- Digilent JTAG USB to Micro-B cable
- AC power adapter (12 VDC)
- TeraTerm Pro terminal program, or equivalent terminal program [\[Ref 7\]](#)
- USB-UART drivers from Silicon Labs

Hardware Test Board Setup

This section details the hardware setup and use of the terminal program for running the BIST application. It contains step-by-step instructions for board bring-up.

ZC706 Evaluation Board Setup

To set the ZC706 jumpers and switches, verify the switch and jumper settings are set as listed in [Figure 2-2](#).

Note: To run the BIST, SW4 must be set to 01 if using the USB Type-A to Micro-B cable provided in the kit, or to 10 if using the Platform Cable USB (II) JTAG cable.

Note: For this application, the board should be set up as a stand-alone system, with power coming from the cord and AC adapter that comes with the ZC706 evaluation kit.

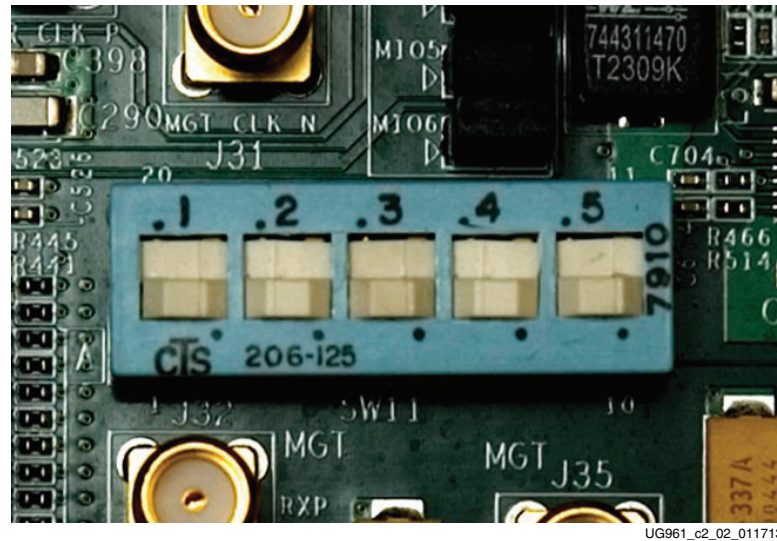
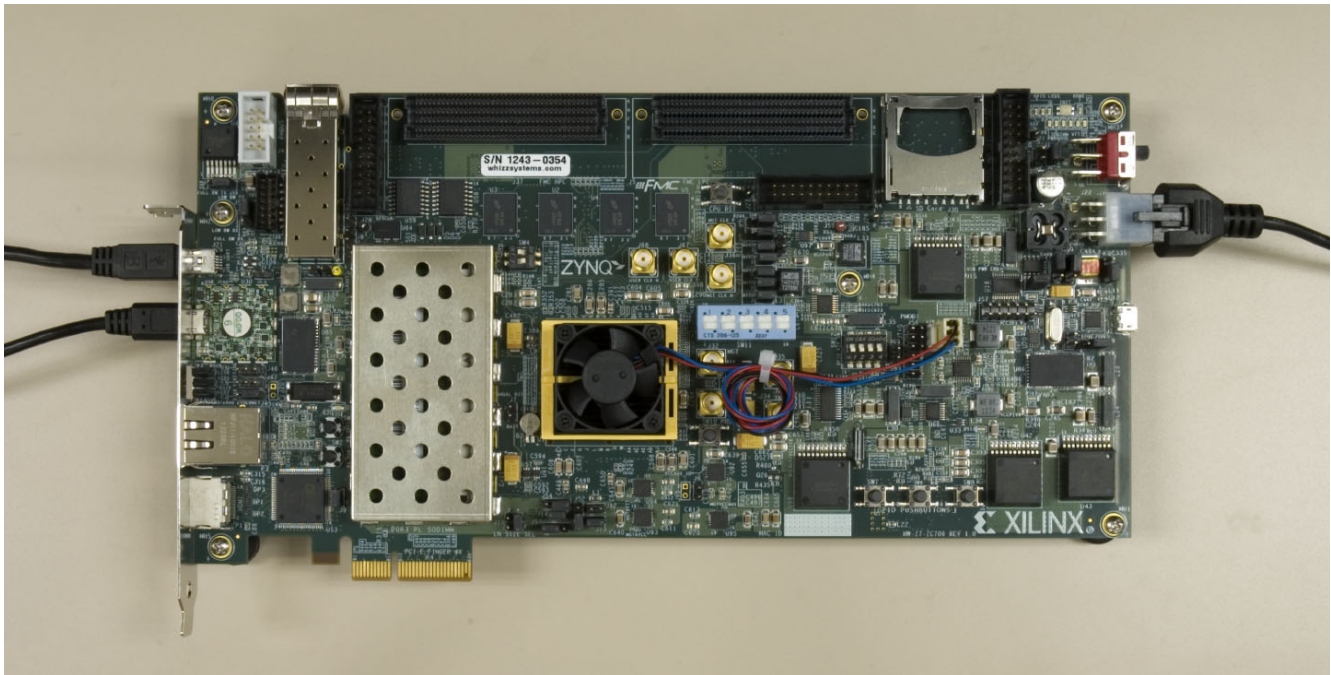


Figure 2-2: Switch Settings on the ZC706 Board

Hardware Bring-Up

This section details the steps for hardware bring-up.

1. With the board switched off, plug a USB Mini-B cable into the UART port of the ZC706 board and your control PC.
2. With the board switched off, plug the Digilent JTAG cable into the JTAG port of the ZC706 board and your control PC.



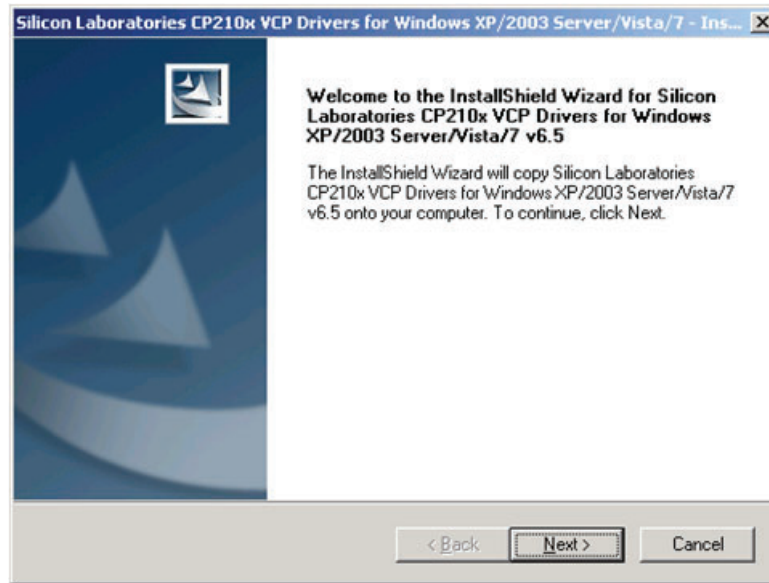
UG961_c2_03_010813

Figure 2-3: ZC706 Board with the UART and Power Cables Attached

3. Install the power cable 12V stand-alone power supply (included).
4. Switch the ZC706 board power to ON.

Install the Silicon Labs Driver

1. Run the downloaded executable UART-USB driver file, listed in [Built-In Self-Test Setup Requirements, page 10](#). This enables UART-USB communications with a control PC (see [Figure 2-4](#)).



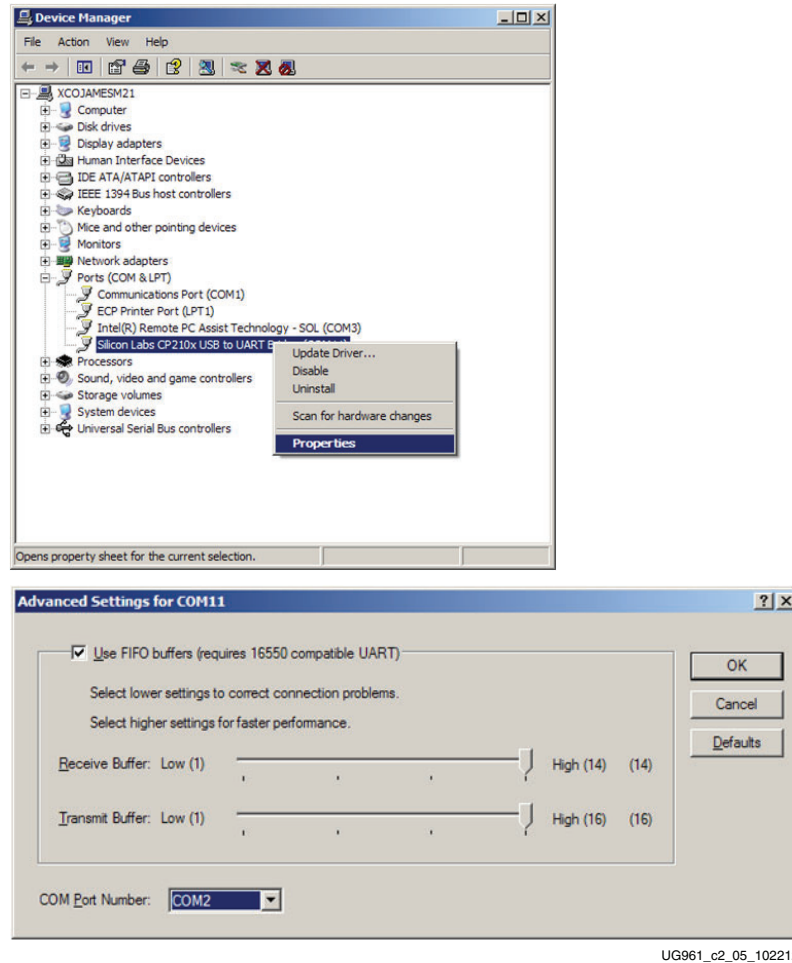
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Figure 2-4: UART Cable Driver Installation

2. Set the USB-UART connection to a known **PORT** in the Device Manager.
3. Right-click **My Computer** and select **Properties**.
4. Select the **Hardware** tab. Click the **Device Manager** button (Windows 7).
5. Click **PORTS** (Windows 7).
6. Find the **Silicon Labs** device in the list, right-click it. Select **Properties**.
7. Click the **Port Settings** tab and the **Advanced...** button.
8. Select an open COM port between COM1 and COM4.

Note: Steps and diagrams refer to using a Windows XP or Windows 7 control PC.

Figure 2-5 shows the steps for setting the USB-UART Port.



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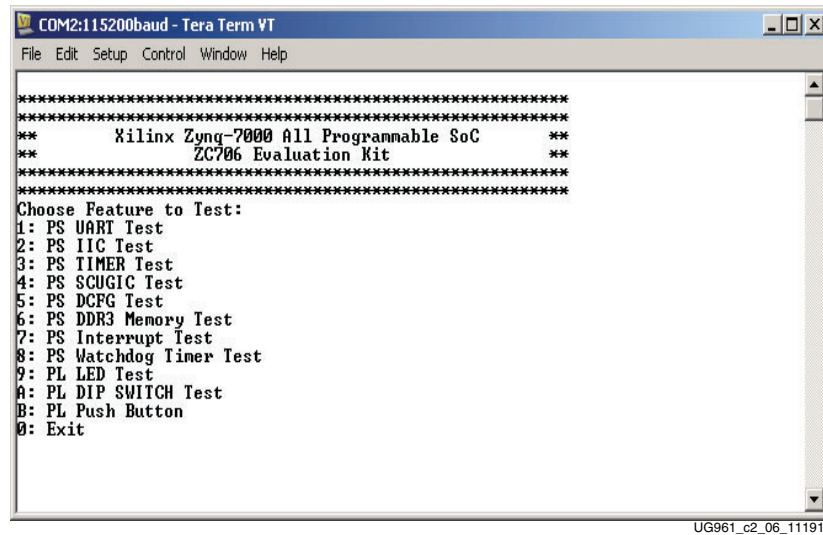
Figure 2-5: Select the Port Settings after Installing the Silicon Labs Driver

Unzip the Application Folder

1. Go to xilinx.com/zc706 and download the latest version of the ZC706 BIST design files.
2. Unzip the folder to your C: / drive.

Run the BIST Application

1. Start the installed terminal program.
2. Click **Setup > Serial Port...** and set Baud rate to 115200, parity to none, data bits to 8, and stop bits to 1.
3. Run the script file in C:\zc706_bist\ready_for_download\zc706_bist.bat (see Figure 2-6).



```
COM2:115200baud - Tera Term VT
File Edit Setup Control Window Help
*****
*****
**      Xilinx Zynq-7000 All Programmable SoC      **
**              ZC706 Evaluation Kit              **
*****
*****
Choose Feature to Test:
1: PS UART Test
2: PS IIC Test
3: PS TIMER Test
4: PS SCUGIC Test
5: PS DCFG Test
6: PS DDR3 Memory Test
7: PS Interrupt Test
8: PS Watchdog Timer Test
9: PL LED Test
A: PL DIP SWITCH Test
B: PL Push Button
0: Exit
```

UG961_c2_06_111912

Figure 2-6: The ZC706 BIST Menu

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard non-volatile storage, see resources at xilinx.com/zc706 listed under the **Docs & Designs** tab.

Getting Started with the ZC706 PCIe Targeted Reference Design

Introduction

The Zynq-7000 PCIe® Targeted Reference Design (TRD) expands the Zynq-7000 All Programmable SoC ZC702 Base TRD ([UG925](#), *Zynq-7000 All Programmable SoC ZC702 Base Targeted Reference Design User Guide*) by adding PCI Express® communication with a PCIe host system at PCIe x4 GEN2 speed. In the ZC702 Base TRD, the input of the video processing pipeline is generated by a test pattern generator in the FPGA logic. In this design, the input of the video processing pipeline is generated by an application on the PCIe host computer at 1080p60 resolution and transmitted to the ZC706 board through PCIe. The data is processed by video pipeline and passed back to the PCIe host system through PCIe. As the full 1080p60 video stream only takes up around 4 Gb/s, an additional data generator and a checker are implemented and connected to channel 1 of PCIe DMA, showcasing the maximum PCIe x4 GEN2 bandwidth achieved by the hardware.

The Zynq-7000 PCIe TRD demonstrates the following components working together:

- PCIe Endpoint (x4 GEN2)
- High speed serial transceivers
- High speed multichannel DMA interfacing to PCIe Endpoint
- Zynq-7000 Processing System (PS)
- Video DMA (VDMA) and Sobel filtering
- HDMI based display controller

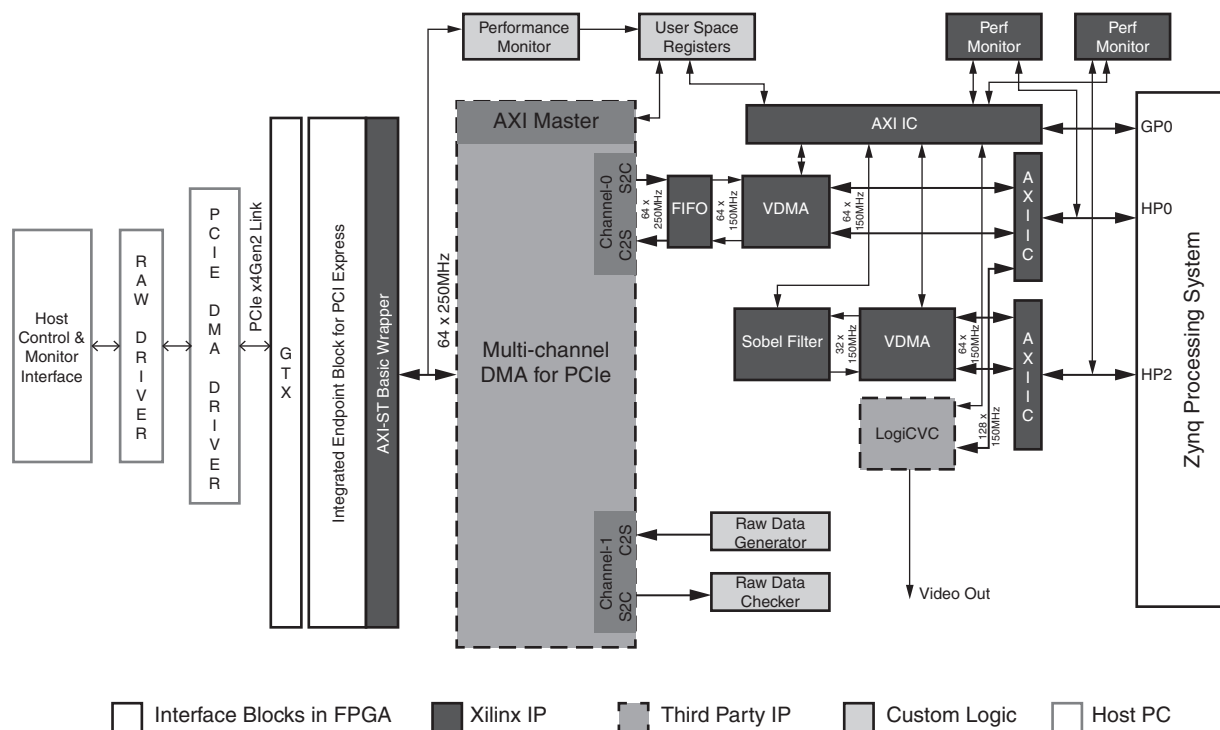


Figure 3-1: Zynq-7000 PCIe TRD Block Diagram

The design is a PCI Express based video processing card demonstrating the following capabilities:

- PCIe based connectivity demonstration
 - PCI Express block of ZC7Z045 used in x4 GEN2 configuration
 - PCI Express compatible high performance low latency multichannel DMA from third party vendor Northwest Logic [Ref 8].
 - Performance demonstration using traffic generator and checker running on FPGA hardware and PCIe host software containing PCIe root port
- ARM Cortex-A9 core processor processing and offload demonstration
 - Zynq-7000 AP SoC as an off-load device to process video data—The TRD provides an example with the Sobel filter in the Zynq-7000 AP SoC programmable logic (PL).
 - HDMI based display controller from third party vendor
 - Cortex-A9 in Zynq-7000 as a co-processor processing video data
 - An example design showing independent memory management in the PCIe host system and Cortex-A9 PS.

Key Components

The PCIe TRD features the following components:

- PCI Express v2.1 compliant x4 Endpoint operating at 5 Gb/s/lane/direction
 - PCIe transaction interface utilization engine
 - Message signal interrupt (MSI) and legacy interrupt support
- Bus mastering scatter-gather PCIe DMA to offload the PCIe host processor
 - Multichannel DMA
 - AXI4 Streaming interface for data
 - AXI4 interface for register space access
 - DMA performance engine
 - Full duplex operation
 - Independent transmit and receive channels
- Multichannel VDMA with programmable VSIZE and HSIZE
 - AXI4 compliant
 - Optional flush on frame sync
 - Optional frame advancement on error
- Multilayer display controller
 - Alpha blending, transparency, and move around support
 - Continuous switching mode support
- Sobel filter
 - AXI4 Stream interface
 - AXI4 Control interface
 - Supports image size up to 1080p
- Java based GUI running on the PCIe host system
 - Test control panel
 - PCIe performance monitoring
- A QT based GUI running on Zynq-7000 PS
 - Monitors power and die temperature
 - Zynq-7000 processing system's HP0 and HP2 performance numbers

- CPU utilization

Data Flow

The TRD shows how the Zynq-7000 platform can be used as an off-load engine to the PCIe host machine it is connected to.

Video Processing and Offload Demonstration on Channel 0 of PCIe DMA

The user application in the PCIe host system repeatedly generates video frames of size 1920 x 1080 pixels containing 8 color bars. Software on the PCIe host system manages channel 0 of PCIe DMA to transmit the video stream from the PCIe host over x4 GEN2 PCIe links to the Zynq-7000 ZC706 board. PCIe DMA translates the stream of PCIe video data packets into AXI streaming data, which is in turn connected to a video DMA (VDMA). Software running on the Cortex-A9 processor manages the AXI VDMA and transfers the raw video frames into the PS DDR3 memory. The Sobel filter in the PL reads the image using another VDMA, performs edge detection on the raw image, and sends the data back to PS DDR3. The processed data in PS DDR3 can either be transferred back to PCIe host system using channel 0 of card-to-system (C2S) interface of PCIe DMA or be displayed on the monitor using the LogiCVC display controller. Due to limitations of the PS DDR3 bandwidth, the same data cannot be displayed and sent back to PCIe host system simultaneously. As in the Base TRD, this design also demonstrates hardware based Sobel filter for video processing.

Generator and Checker Demonstration on Channel 1 of PCIe DMA

A generator and checker on channel 1 of PCIe DMA allow the RX and TX paths to run independently. The hardware generator in the PL fabric generates data packets with an incremental sequence pattern. The software checker running on the PCIe host system verifies the incremental sequence pattern generated by the hardware generator. Independently, the driver running on the PCIe host system generates a stream of incremental data which is transferred through PCIe link by NWL PCIe DMA to the checker implemented in the PL fabric.

Hardware Test Setup

This section describes how to set up the ZC706 board, control computer, host computer, and software for the Zynq™-7000 PCIe® Targeted Reference Design.

Additional Materials

User-supplied materials include:

- Monitor supporting 1080p
- Two personal computers (PCs). See [Computer Requirements](#).
- USB mouse (for use with the ZC706 board)

Computer Requirements

Running the Zynq-7000 PCIe TRD requires two PCs.

Control PC

The TRD requires an Intel processor-based laptop or desktop PC running the Windows 7 operating system. The computer must have an SD memory card receptacle, and one USB port to communicate with the ZC706 board.

Required Software

The software listed here must be installed on the control computer:

- ISE Design Suite: System Edition.
 - Communications drivers and terminal program. See [UG963](#), *Zynq-7000 All Programmable SoC ZC706 PCI Express Targeted Reference Design User Guide*, Appendix A for details.

PCIe Host System Computer

An Intel processor-based desktop PC running Fedora Core 16 Linux operating system is required for the PCIe host system. The computer must have a PCIe v2.0 slot where the ZC706 board is installed in the open chassis of this computer.

Recommended Motherboards

The recommended PCI Express GEN2 PC system motherboards are:

- Sandy Bridge motherboard
- Ivy Bridge motherboard

Programming the ZC706 Board

The XC7Z045 AP SoC is configured from a bitstream in a 2 x 128 Mb Quad-SPI flash memory. This bitstream must first be loaded in the Quad-SPI flash memory from the SD card plugged into J30 on the ZC706 board.

Files for configuring the Zynq-7000 PCIe TRD are compiled in `zc706_pcie_trd.bin` which contains the `zynq_fsb1.elf` bitstream and `u-boot.elf` bitstream along with the Linux kernel, Linux file system image files, and Linux device tree binary files.

Extracting the Project Files

The Zynq-7000 PCIe Targeted Reference Design files are located in `zc706-pcie-trd-rdf0287.zip`. This file is available for download online at www.xilinx.com/zc706 (listed under the **Docs & Designs** tab).

To extract the files:

1. Download `zc706-pcie-trd-rdf0287.zip` to a working directory on the control computer.
2. Unzip the files contained in `zc706-pcie-trd-rdf0287.zip`.

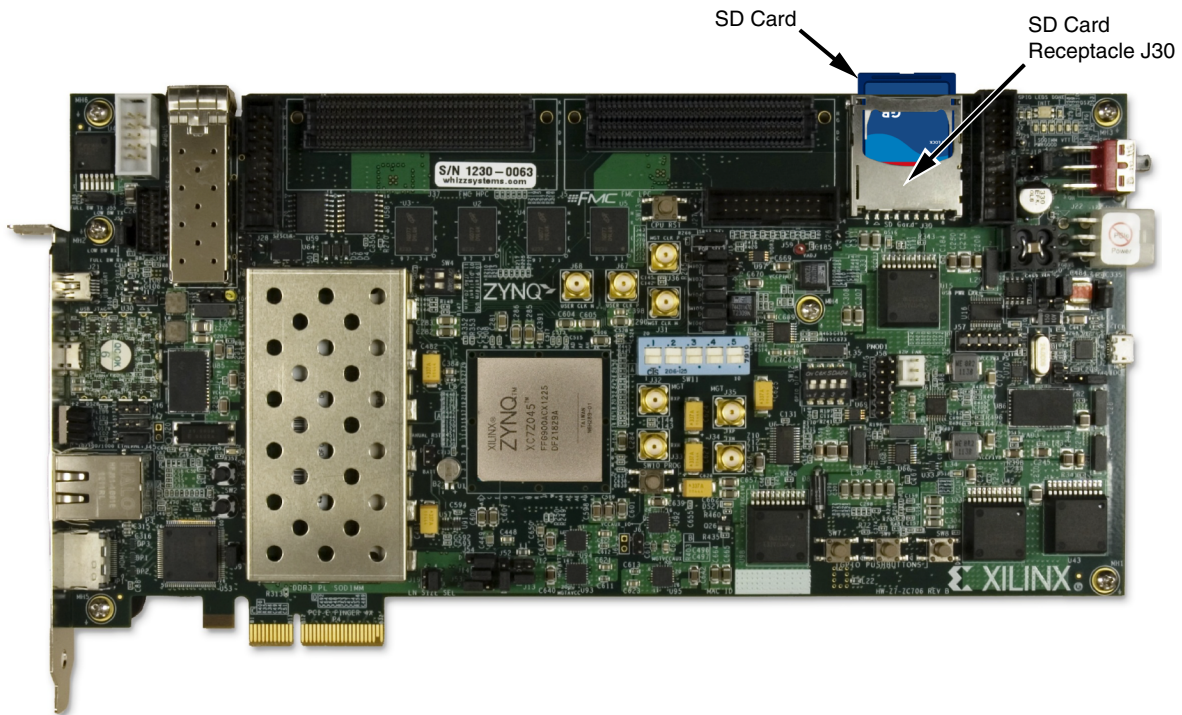
Programming the SD Card

On the control computer:

1. Plug the SD card into the SD card receptacle.
2. Navigate to the working directory `zc706-pcie-trd-rdf0287/prog_qspi` and copy `BOOT.bin`, `zc706_pcie_trd.bin`, `devicetree.dtb`, `devicetree_qspi.dtb`, `uramdisk.image.gz`, `uImage`, and `init.sh` to the SD card.

The `BOOT.bin` file enables the PS to boot in the SD boot mode. The `zc706_pcie_trd.bin` file contains the TRD bitstream. The remaining files are required for Linux boot-up.

3. Unmount and remove the SD card from the computer and insert it into the SD card receptacle on the ZC706 board (Figure 3-2).



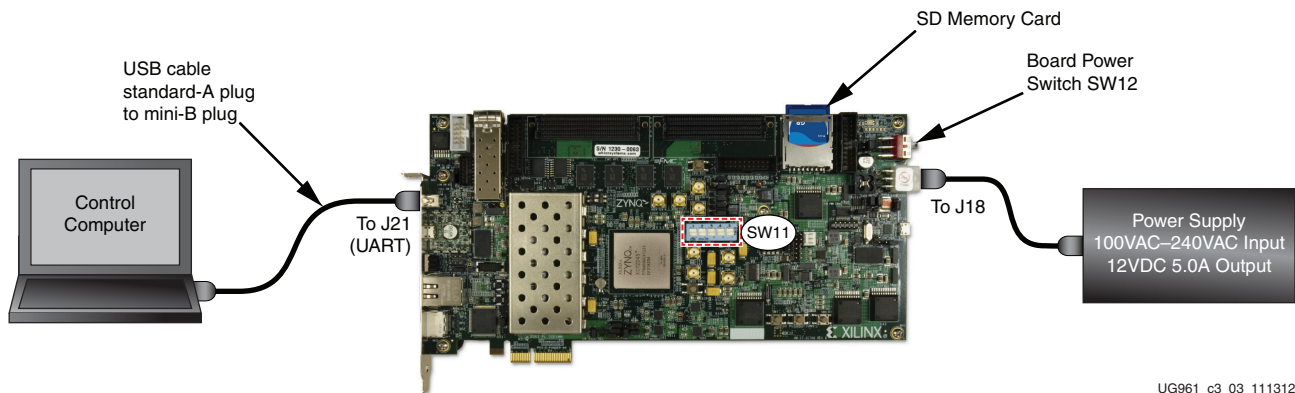
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Figure 3-2: SD Card Location

Programming the Quad-SPI Flash Memory

This procedure programs the Quad-SPI flash memory with files from the SD card to run the Zynq-7000 PCIe TRD.

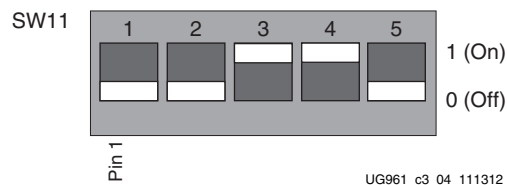
1. Complete the communications setup. (See [UG963](#), *Zynq-7000 All Programmable SoC ZC706 PCI Express Targeted Reference Design User Guide, Appendix A* for details.)
2. Power off the ZC706 board (SW12).
3. Verify the SD card is plugged into receptacle J30 as shown in [Figure 3-3](#).
4. Connect the ZC706 board to the control computer and power supply as shown in [Figure 3-3](#).



UG961_c3_03_111312

Figure 3-3: ZC706 Board Programming Setup

- Set DIP switch SW11 as shown in [Figure 3-4](#).



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Figure 3-4: SW11 SD Boot Mode Settings

- Power ON the control computer and start TeraTerm Pro using **115200** bits/s, **8** data bits, **None** parity, **1** stop bit, **None** flow control.
- Power ON the ZC706 board (SW12). The `init.sh` script in the SD card loads the Quad-SPI flash memory with `zc706_pcie_trd.bin` and the Linux kernel images. Initialization progress is shown on the TeraTerm Pro display ([Figure 3-5](#)).

Four commands are executed by `init.sh`:

```
zynq>flashcp -v zc706_pcie_trd.bin /dev/mtd0
```

```
zynq>flashcp -v uImage /dev/mtd1
```

```
zynq>flashcp -v devicetree_qspi.dtb /dev/mtd2
```

```
zynq>flashcp -v uramdisk.image.gz /dev/mtd3
```

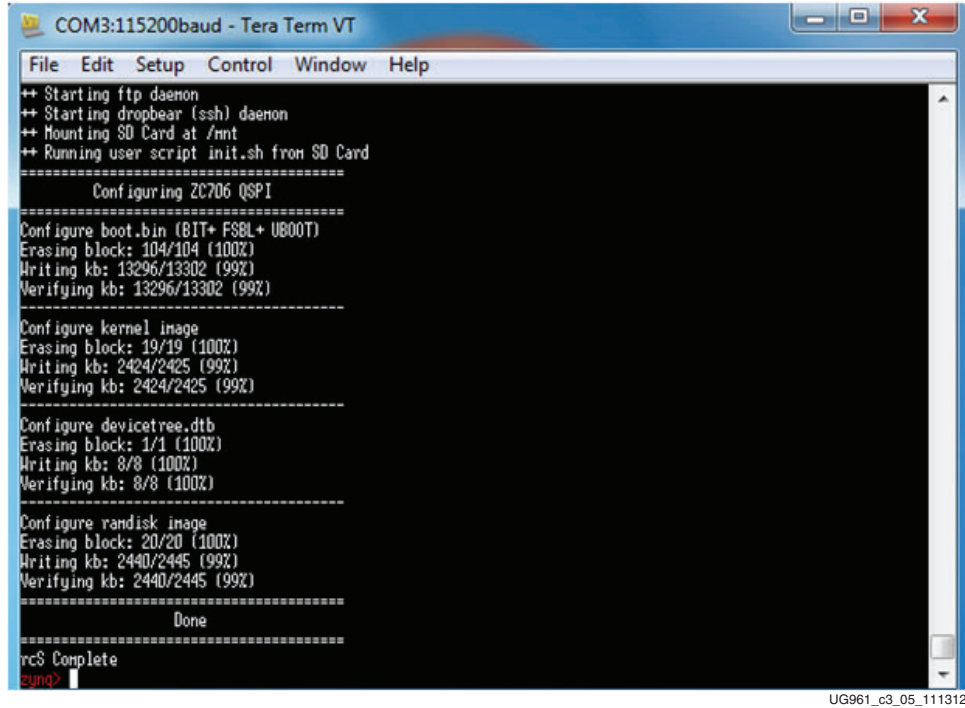



Figure 3-5: Initialization Progress of the init.sh Script

8. Initialization is complete when the `zynq>` prompt appears on the TeraTerm Pro display.
9. Navigate to the `zc706-pcie-trd-rdf0287/sd_image` folder and copy `qt_lib.img`, `init.sh`, `zynq_pcie_qt.elf`, `zynq_pcie_cmd.elf`, and `zynq_pcie_qt.sh` files to the SD card used to program the QSPI device. These files are required for loading the Zynq-7000 PCIe TRD. Insert the SD card into the SD card slot.
10. Set DIP switch SW11 for Quad SPI boot mode, as shown in Figure 3-6.

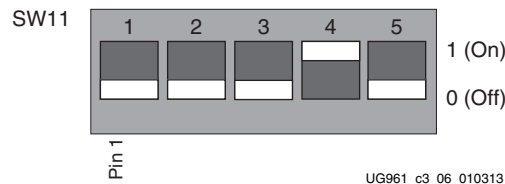


Figure 3-6: SW11 Quad SPI Flash Memory Settings

TRD Demonstration Setup

This section describes hardware bring-up, software bring-up, and using the application GUI.

Installing ZC706 Board in the Host Computer Chassis

When the ZC706 board is used inside a computer chassis power is provided from the ATX power supply peripheral connector through the ATX adapter cable shown in [Figure 3-7](#).

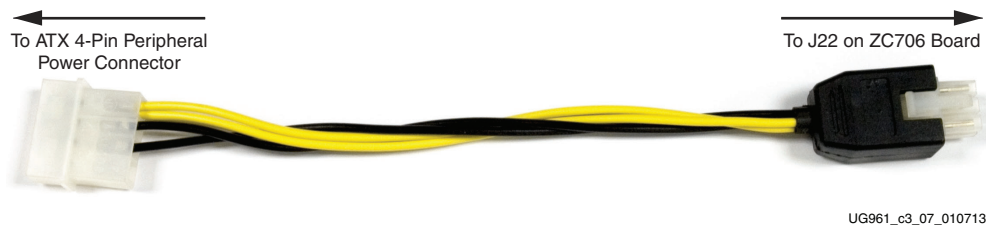


Figure 3-7: ATX Power Supply Adapter Cable

To install the ZC706 board in a computer chassis:

1. Remove all six rubber feet and standoffs from the ZC706 board.
2. Power down the host computer and remove the computer power cord.
3. Open the chassis, select a vacant PCIe expansion slot, and remove the expansion cover at the back of the chassis.
4. Plug the ZC706 board into the PCIe connector at this slot.
5. Install the top mounting bracket screw into the PC expansion cover retainer bracket to secure the ZC706 board in its slot.



IMPORTANT: *The ZC706 board is taller than standard PCIe cards. Ensure that the height of the card is free of obstructions.*

6. Connect the ATX power supply to the ZC706 board using the ATX power supply adapter cable as shown in [Figure 3-8](#).
7. Connect one end of the HDMI cable to the ZC706 HDMI slot (P1) and the other end to the HDMI monitor ([Figure 3-8](#)).
8. Slide the ZC706 board power switch SW12 to the ON position.

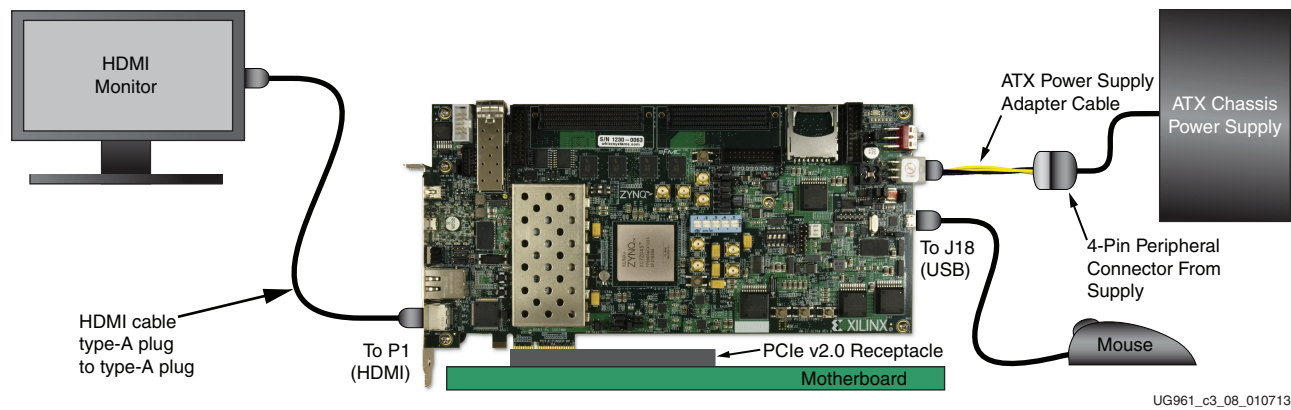


Figure 3-8: ZC706 Board TRD Setup in Host Computer

Installing Device Drivers

Host Computer Bootup

The procedures listed in this section require Linux super user access on the host computer. When using the Fedora 16 LiveDVD, super user access is granted by default. If not using the Fedora 16 LiveDVD, contact your system administrator for super user access.

If Fedora 16 is installed on the host computer hard disk, boot as a root-privileged user.

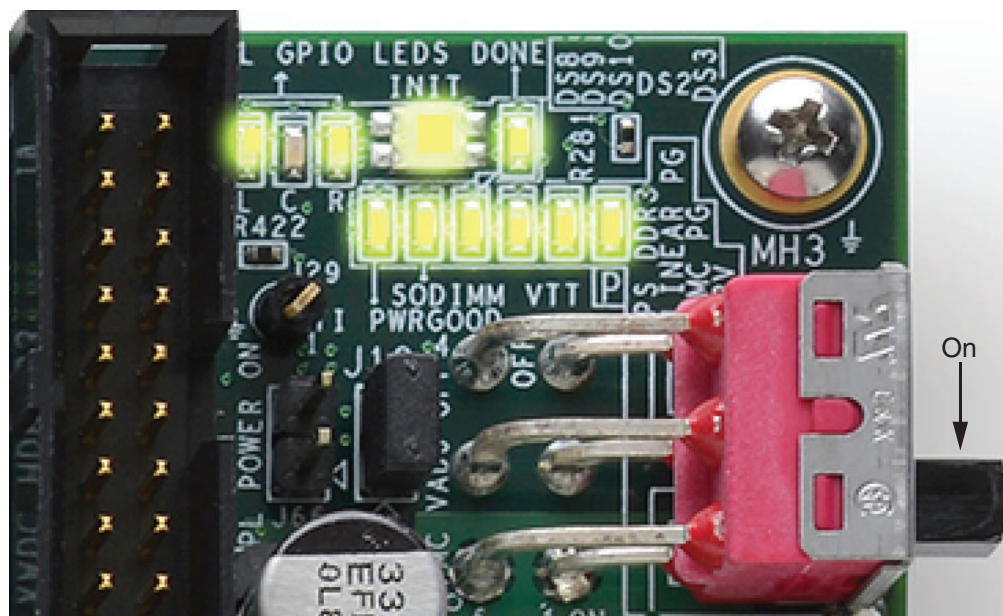
If Linux is not installed, place the Fedora 16 LiveDVD in the host computer CD-ROM drive and restart the computer.

The Fedora 16 Live Media is for Intel-compatible PCs and contains a complete, bootable 32-bit Fedora 16 environment with the proper packages installed for the TRD demonstration. The PC boots from the CD-ROM drive and logs into a liveuser account that has the kernel development root privileges required to install and remove device driver modules.



IMPORTANT: The BIOS boot order must be set so that the CD-ROM drive is the first drive in the boot order. To set the boot order, power on the computer and press the **DEL** or **F2** key. Set the boot order and save the change.

1. Switch SW12 on the ZC706 board to the ON position (as shown in [Figure 3-9](#)).



UG961_c3_09_011713

Figure 3-9: SW12 in the ON Position

- Power on the PCIe host system. The Zynq-7000 PCIe TRD provides PCIe status on the GPIO LEDs near the ZC706 board power switch (Figure 3-9). The LEDs that should glow are listed in Table 3-1 (L is the left-most LED in row 1, and LED1 is the left-most LED in row 2.)

Table 3-1: LEADS Showing PCIe Status

Row	Labels					
	L	C	R	INIT	DONE	DS10
Top Row	Green -BLINKING-	Off	Green	Green	Green	Off
	LED1	LED2	LED3	LED4	LED5	LED6
Bottom Row	Green	Green	Green	Green	Green	Green

LED R and L should be ON and LED C should be OFF. The LEDs represent the following:

- LED R- PCIe link up
- LED C - User reset from PCIe IP
- LED L: User clock heartbeat LED

The images in Figure 3-10 are seen on the monitor during boot up. On the HDMI monitor connected to the ZC706 board, a Qt-based application appears that shows device power and temperature.

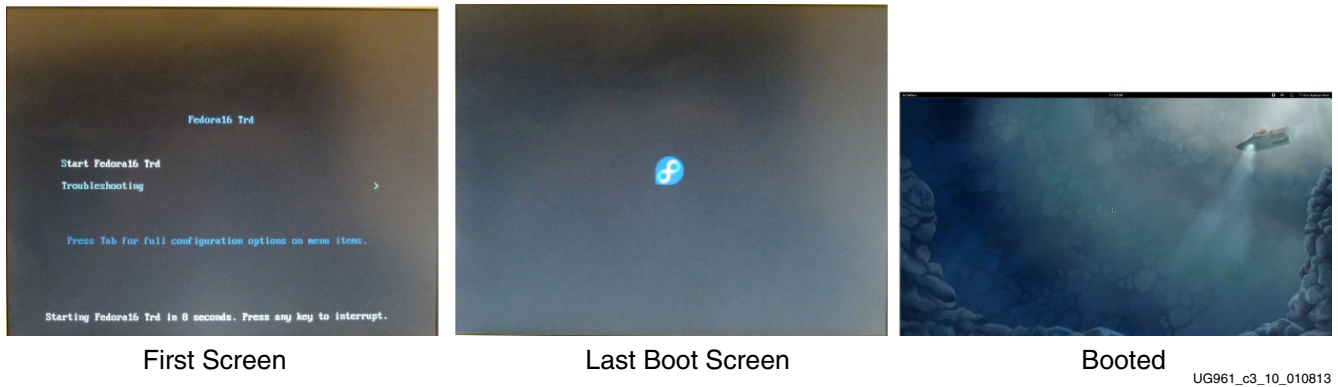


Figure 3-10: Fedora 16 LiveDVD Boot Sequence

- Download `zc706-pcie-trd-rdf0287.zip` from www.xilinx.com/zc706 and copy it to specific `/tmp` folder of PCIe host PC. Unzip the file. Change permission by typing `chmod 755 -R zc706-pcie-trd-rdf0287` on a terminal so the files have execution permission. Double click on the copied `zc706-pcie-trd-rdf0287`. The screen capture in Figure 3-11 shows the content of the `zc706-pcie-trd-rdf0287` folder.

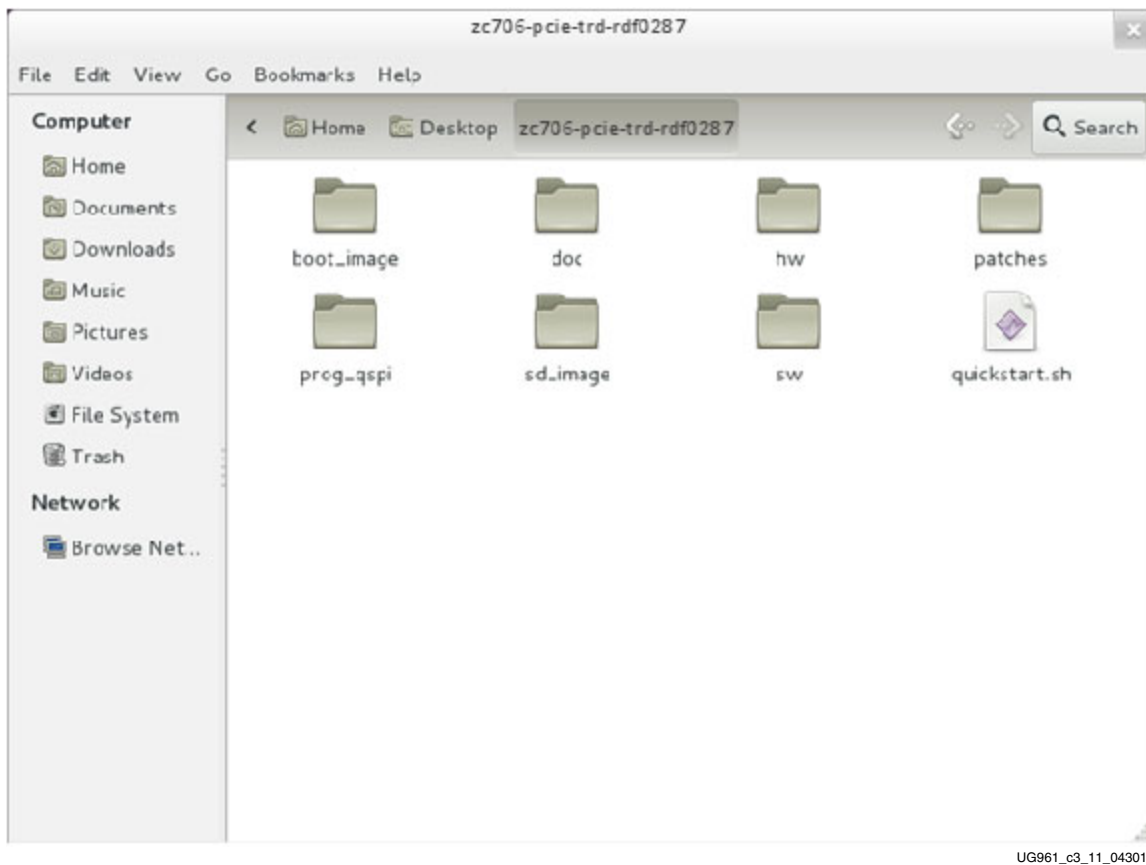
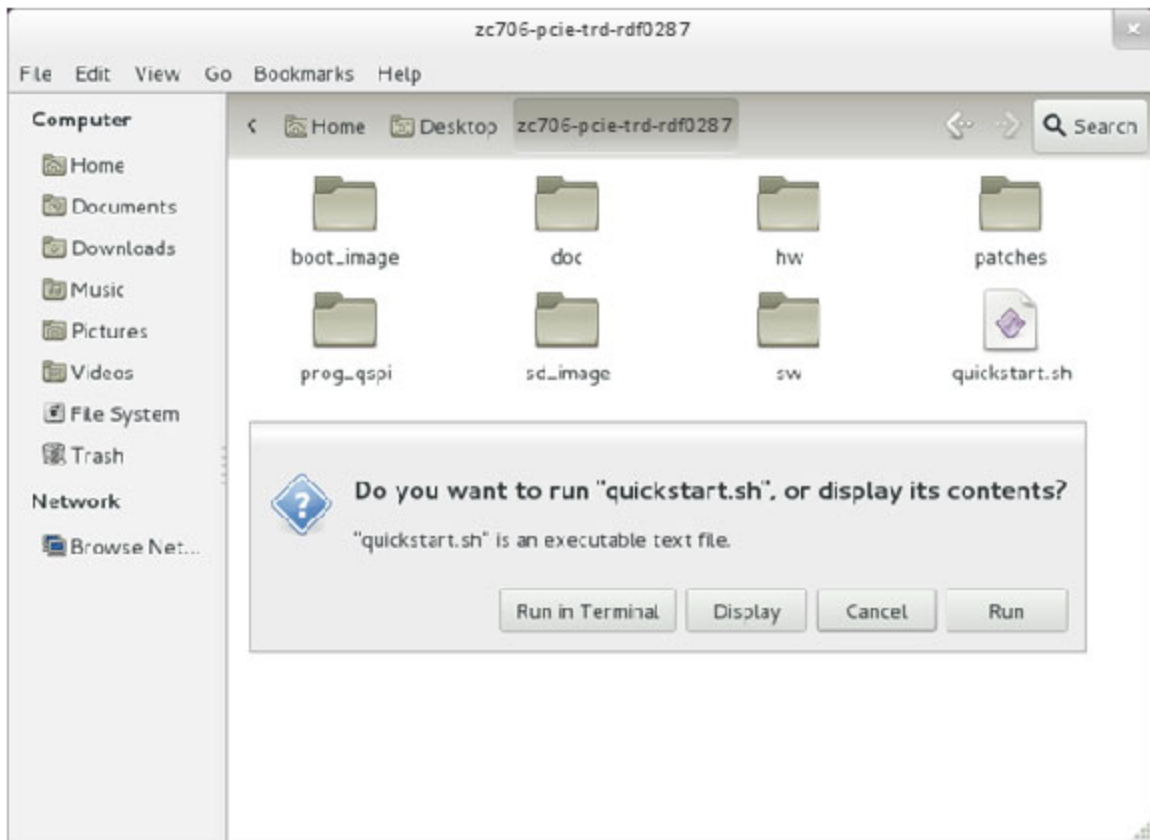


Figure 3-11: Directory Structure of z7_pcie_trd

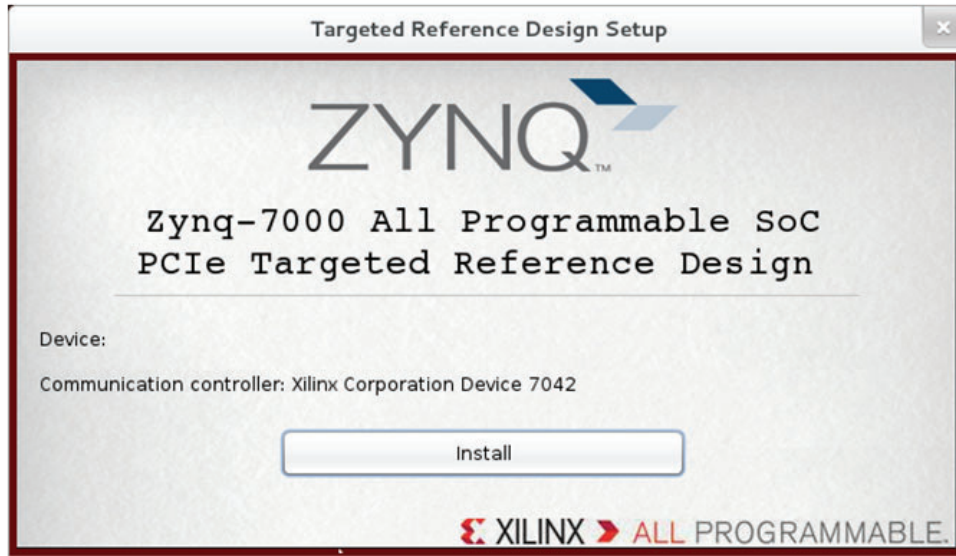
4. Double click on the `quickstart.sh` script. This script sets proper permission and invokes the driver installation GUI. Click **Run in Terminal**.



UG961_c3_12_043013

Figure 3-12: Running Quickstart Script

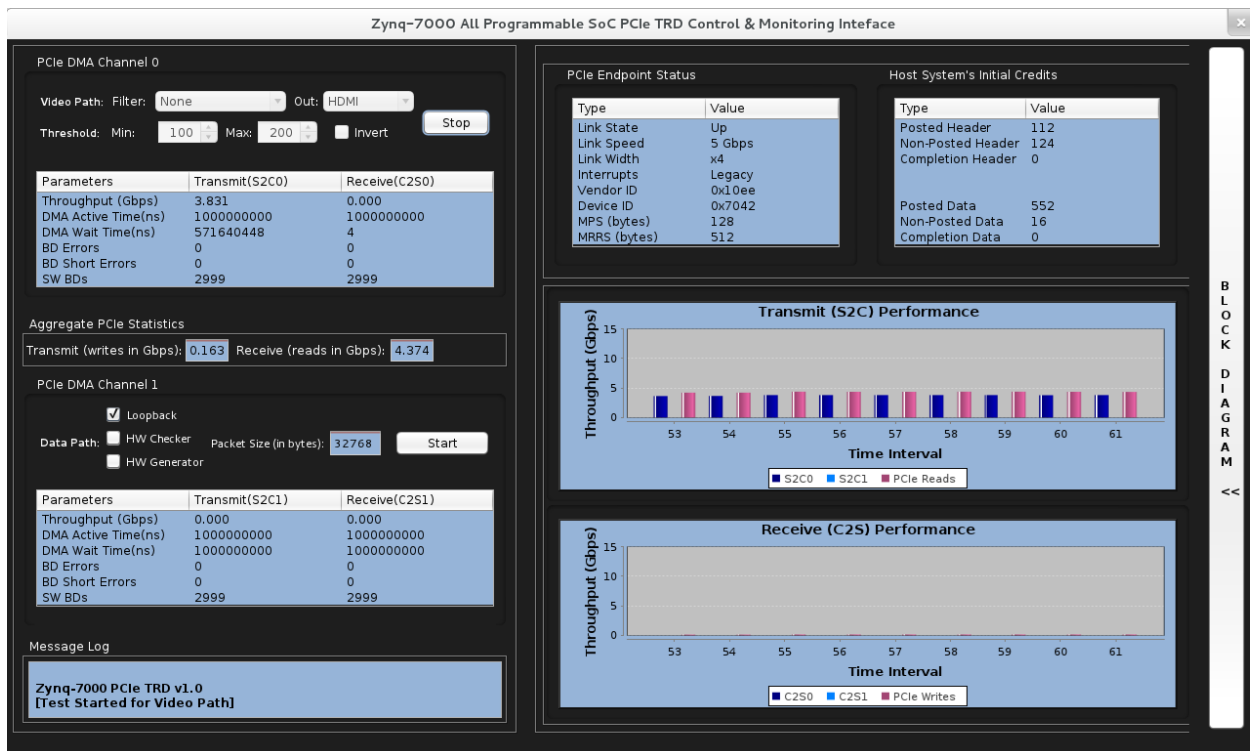
5. The GUI with driver installation option pops up as shown in [Figure 3-12](#). The step installs all the software necessary for the host system to control, generate, and receive PCIe traffic to and from the ZC706 board and monitor performance. Click **Install**.



UG961_c3_13_111312

Figure 3-13: Install Dialog Box of Zynq-7000 PCIe TRD

6. After installing the Video/Raw performance mode driver, the control and monitor user interface pops up as shown in Figure 3-14. The control pane shows control parameters such as Sobel Filter and Video Out selection modes.



UG961_c3_14_041013

Figure 3-14: Video/Raw Performance Mode

- Click the **Start** button in the Video Path panel to start the PCIe host system generating a 1080p60 video stream and sending it over to the ZC706 board through PCIe. The video stream is processed and displayed on the HDMI monitor or sent back to the host through PCIe, based on the test mode selected in the Video Out menu. The Performance Plots tab shows the system-to-card (S2C) and card-to-system (C2S) PCIe performance numbers.

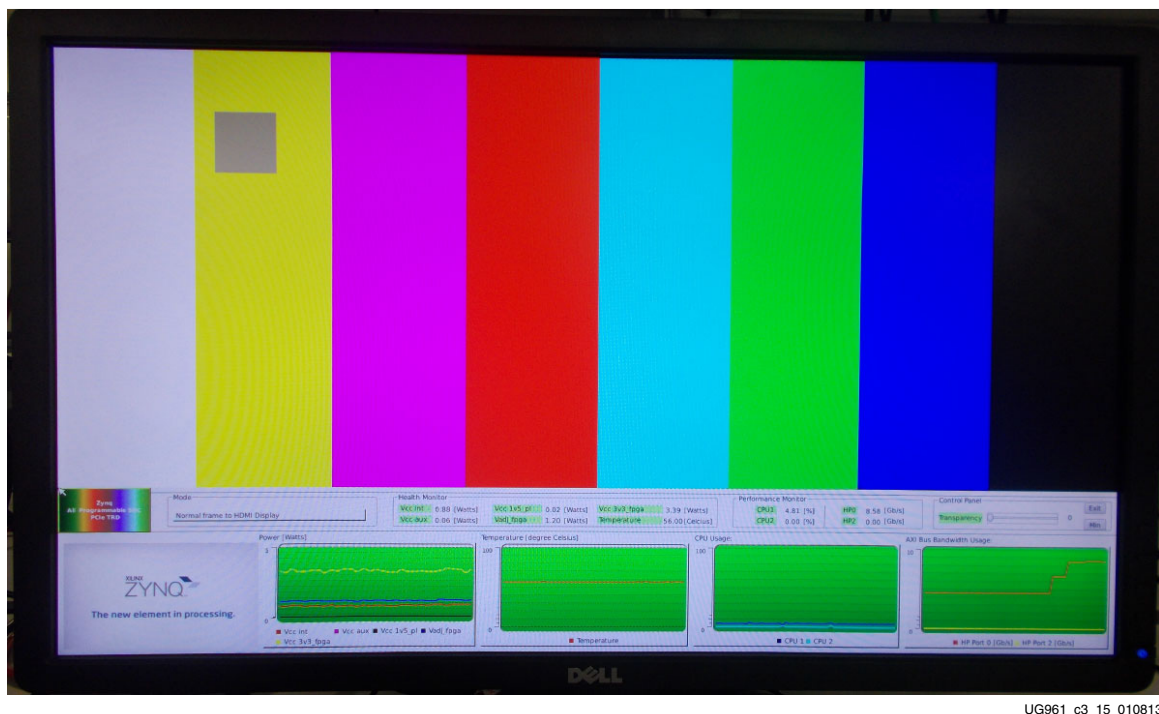
You can select various test modes from the Sobel Filter drop-down menu:

- Select option **None** to display the frames on the monitor without Sobel.
- Select option **Sobel-HW** to display the frames on the monitor with HW Sobel.
- Select option **Sobel-SW** to display the frames on the monitor with SW Sobel.

You can select various test modes from the Video Out drop-down menu:

- Select option **HDMI** to display Sobel data on HDMI monitor.
- Select option **PCIe Host** to send data back to the PCIe host system.

For option Sobel Filter: **None** and Video Out: **HDMI**, video data from PCIe host system is directly sent to the display without being processed by the edge detection Sobel filter. A color bar pattern appears on the display as shown in [Figure 3-15](#) for this option.



UG961_c3_15_010813

Figure 3-15: HDMI Display for Color Bar Display

- For the options Sobel Filter: **Sobel-HW** and Video Out: **HDMI**, video data from the PCIe host system is directly processed by the edge detection Sobel filter in the PL based on

Max and **Min** threshold values selection provided through the host GUI, then sent to the display. Edges of the color bar pattern appear on the display as shown in [Figure 3-15](#) for this option without invert option. Optionally, the Sobel output video can be inverted by selecting **Invert** check box on the GUI.



UG961_c3_16_010813

Figure 3-16: HDMI Display for Sobel Output Display

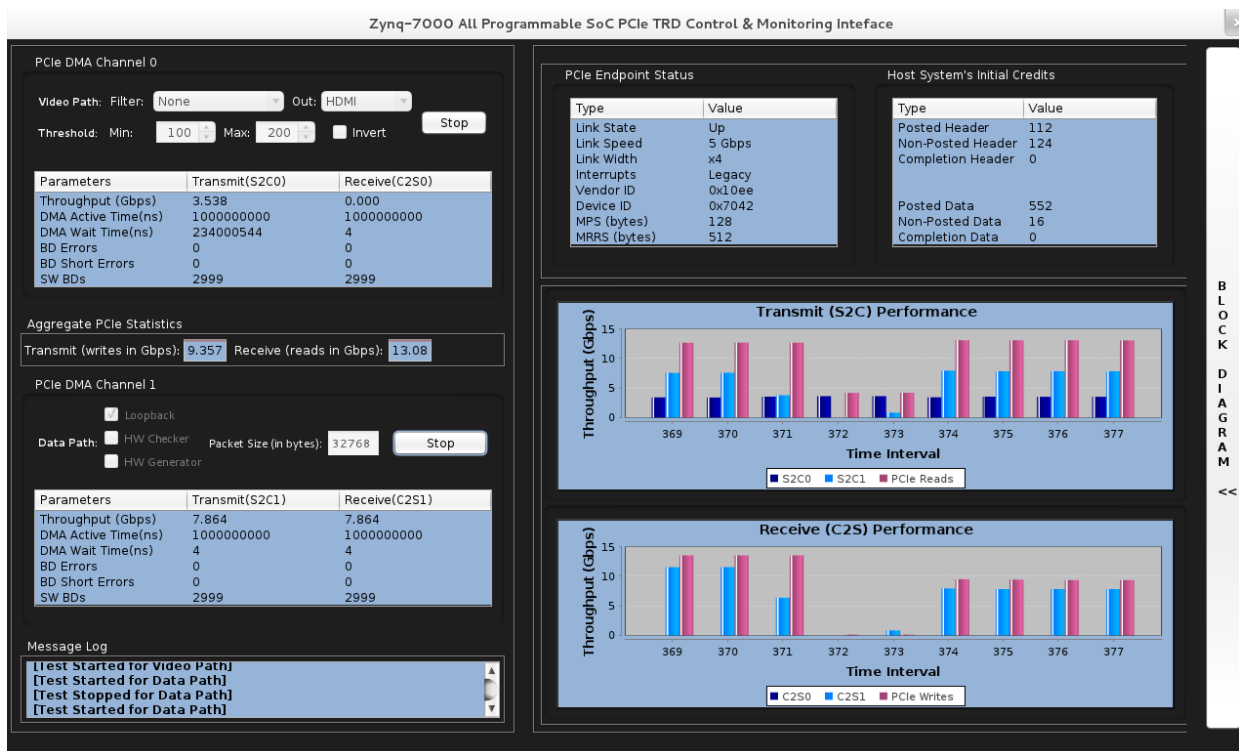
For option Sobel Filter: **Sobel-SW** and Video Out: **HDMI**, video data from the PCIe host system is directly processed by the edge detection Sobel filter in the PS, then sent to the display. Edges of the color bar pattern appear on the display.

For option Video Out: **PCIe Host**, video data from PCIe host system is processed by Sobel filter in the PL or PS depending on mode selected in Sobel Filter, then sent back to the PCIe host system through PCIe. The data is not sent to the display. Sobel Filter: **None** is not a supported option when Video Out is set to **PCIe Host**.

The Qt GUI monitors the power of the device voltage rails and die temperature. The CPU utilization and PS HP port 0 and HP port 2 performance numbers are also periodically plotted. When the user selects Sobel Filter: **None** HP port 0 performance becomes 8 Gb/s and HP port 2 port performance becomes 0 Gb/s. When the user selects Sobel Filter: **Sobel-HW** both HP port 0 and HP port 2 performance is close to 8 Gb/s. When you select Sobel Filter: **Sobel-SW**, the CPU2 performance becomes 100%, HP port 0 performance becomes close to 8 Gb/s, and HP port 2 performance becomes 0.

- As noted in the discussion above, because a single HD stream of video data is insufficient to saturate available PCIe x4 GEN2 bandwidth, datapath 1 can be turned on

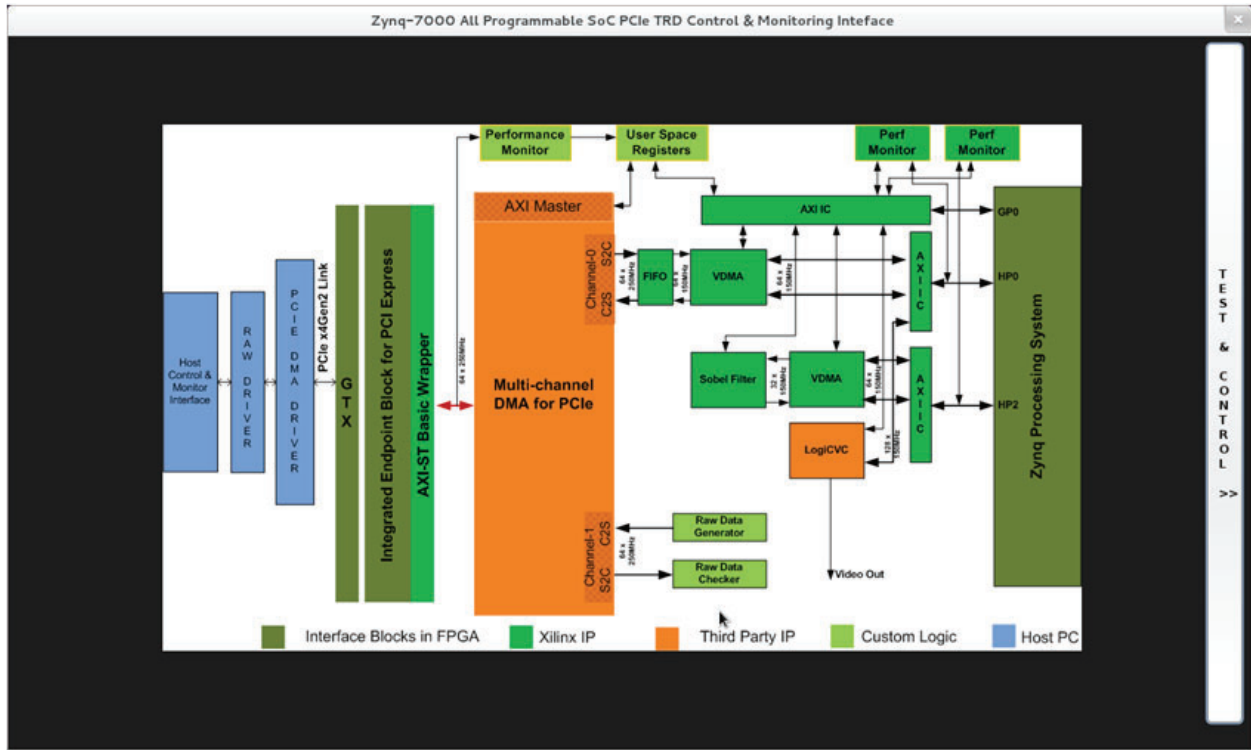
to add additional PCIe traffic. Click on the **Start** button in the Data Path-1 panel to generate additional traffic. On this path, the user can vary packet sizes and see performance variation accordingly. Total PCIe BW is updated in the PCIe statistics panel and the performance plot. The user can select **Loopback**, **HW Generator**, and the **HW Checker** option in the GUI for Data Path-1 (Figure 3-17).



UG961_c3_17_041013

Figure 3-17: Video/Raw Performance Mode Plots

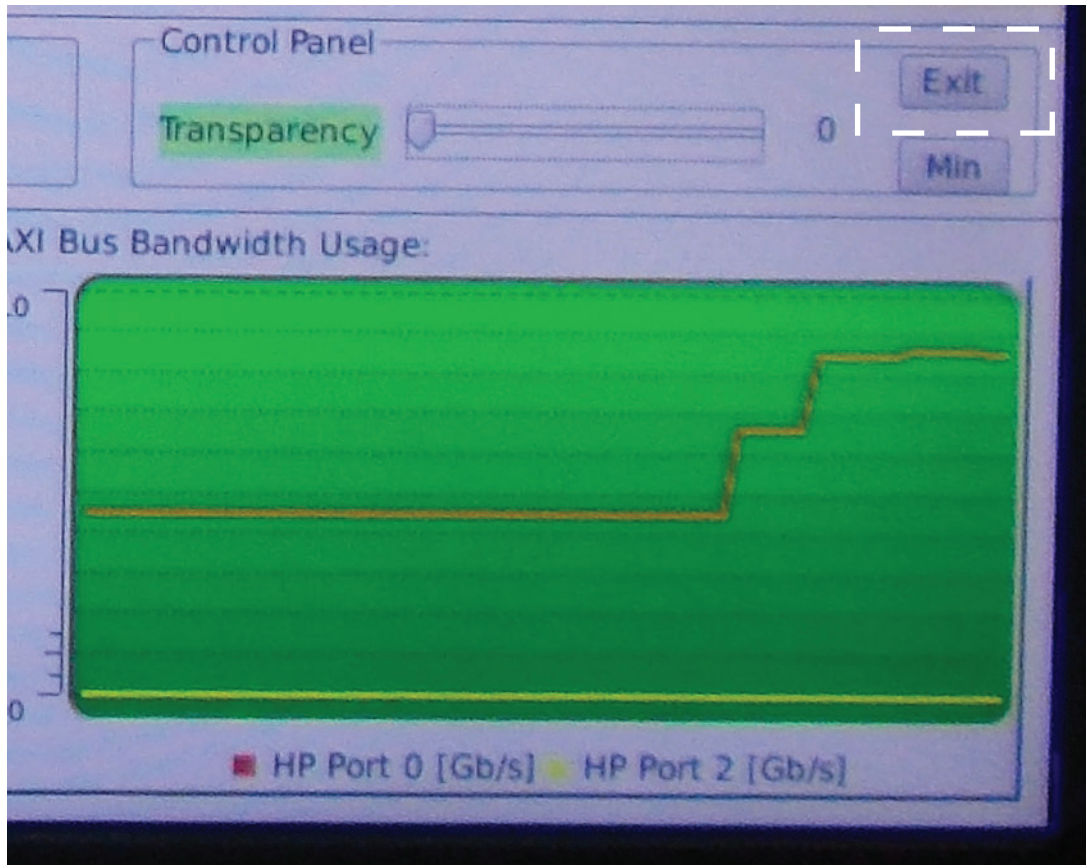
10. Click on the **Block Diagram** option to view the design block diagram as shown in Figure 3-18.



UG961_c3_18_111312

Figure 3-18: Design Block Diagram

11. Exit the Qt GUI by clicking the **Exit** button in the GUI as shown in Figure 3-19.



UG961_c3_19_010713

Figure 3-19: Exiting the Qt GUI

12. Close the GUI.

This process uninstalls the driver on the PCIe host system and opens the landing page of the Zynq-7000 PCIe TRD. Uninstalling the driver requires the GUI to be closed first.

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

<http://www.xilinx.com/support>.

For continual updates, add the Answer Record to your myAlerts:

<http://www.xilinx.com/support/myalerts>.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the [Xilinx Solution Centers](#) for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

The most up to date information related to the ZC706 board and its documentation is available on the following websites.

The Zynq-7000 AP SoC ZC706 Evaluation Kit Product Page:

www.xilinx.com/zc706

The Zynq-7000 AP SoC ZC706 Evaluation Kit Master Answer Record:

<http://www.xilinx.com/support/answers/51899.htm>

These Xilinx documents and sites provide supplemental material useful with this guide:

[DS190](#), *Zynq-7000 Extensible Processing Platform Overview*

[PG164](#), *LogiCORE IP Processor System Reset Module v5.0*

[PG059](#), *LogiCORE IP AXI Interconnect*

[PG020](#), *LogiCORE IP AXI Video Direct Memory Access Product Guide*

[PG054](#) *7 Series FPGAs Integrated Block for PCI Express Product Guide*

[UG585](#), *Zynq-7000 AP SoC Technical Reference Manual*

[UG673](#), *Quick Front-to-Back Overview Tutorial: PlanAhead Design Tool*

[UG798](#), *ISE Design Suite 14: Release Notes, Installation, and Licensing*

[UG821](#), *Zynq-7000 All Programmable SoC Software Developers Guide*

[UG873](#), *Zynq-7000 All Programmable SoC: Concepts, Tools, and Techniques (CTT) A Hands-On Guide to Effective Embedded System Design*

[UG925](#), *Zynq-7000 All Programmable SoC: ZC702 Base Targeted Reference Design User Guide*

[UG926](#), *Zynq-7000 All Programmable SoC: ZC702 Evaluation Kit and Video and Imaging Kit Getting Started Guide*

[UG954](#), *ZC706 Evaluation Board for the Zynq-7000 XC7Z045 All Programmable SoC User Guide*

[UG963](#), *Zynq-7000 All Programmable SoC ZC706 PCI Express Targeted Reference Design User Guide*

Xilinx Zynq-7000 All Programmable SoC website:

www.xilinx.com/products/silicon-devices/soc/zynq-7000/index.htm

Zynq-7000 All Programmable SoC Product Table:

www.xilinx.com/publications/prod_mktg/zynq7000/Zynq-7000-combined-product-table.pdf

Zynq-7000 AP SoC ZC706 Evaluation Kit: www.xilinx.com/ZC706

Xilinx Open Source ARM git Repository: git.xilinx.com/

Using Git: wiki.xilinx.com/using-git

Xilinx ARM GNU Tools: wiki.xilinx.com/zynq-tools

Zynq Linux—Downloading the Kernel Tree: xilinx.wikidot.com/zynq-linux#toc7

Zynq Linux—Configuring and Building the Linux Kernel:

xilinx.wikidot.com/zynq-linux#toc8

Xilinx Open Source Linux: wiki.xilinx.com/open-source-linux

Xilinx Device Tree Generator: xilinx.wikidot.com/device-tree-generator

Xilinx PlanAhead Design and Analysis Tool website:

www.xilinx.com/tools/planahead.htm

More information on the Zynq-7000 AP SoC processor family boards, FMC extension cards, and other kits based on Zynq-7000 architecture is available at this website:

Xilinx Zynq-7000 All Programmable SoC Boards and Kits

www.xilinx.com/products/boards_kits/zynq-7000.htm

Zc702 Base TRD (wiki page)

<http://www.wiki.xilinx.com/Zc702+Base+TRD>

Xilinx Zynq-7000 PCIe Targeted Reference Design wiki page

wiki.xilinx.com/zynq-pcie-trd

References

The following websites provide supplemental material useful with this guide:

1. git: the fast version control system home page: git-scm.com/
2. Device Tree general information: devicetree.org/Main_Page
3. AMBA AXI4-Stream Protocol Specification:
infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ih0051a/index.html
4. PCI-SIG Documentation: www.pcisig.com/specifications
5. Xylon IP Cores

logiCVC-ML Compact Multilayer Video Controller description:

www.logicbricks.com/Products/logiCVC-ML.aspx

logiCVC-ML Compact Multilayer Video Controller data sheet:

www.logicbricks.com/Documentation/Datasheets/IP/logiCVC-ML_hds.pdf

6. Qt Online Reference Documentation. Qt is a toolkit for creating GUIs: doc.qt.nokia.com/
7. Silicon Labs

P210x USB to UART Bridge VCP Drivers:

www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx

USB to UART Bridge:

www.silabs.com/products/interface/usbtouart/Pages/usb-to-uart-bridge.aspx

8. Northwest Logic DMA back-end core: www.nwlogic.com
9. Fedora is a Linux-based operating system used in the development of this TRD.
Fedora project: fedoraproject.org

Warranty

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