

ULTRA LOW CAPACITANCE TVS ARRAY

APPLICATIONS

- ✓ Ethernet - 10/100/1000 Base T
- ✓ Cellular Phones
- ✓ Audio/Video Inputs
- ✓ Personal Digital Assistant (PDA)

IEC COMPATIBILITY (EN61000-4)

- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 24A, 8/20 μ s - Level 2(Line-Ground) & Level 3(Line-Line)

FEATURES

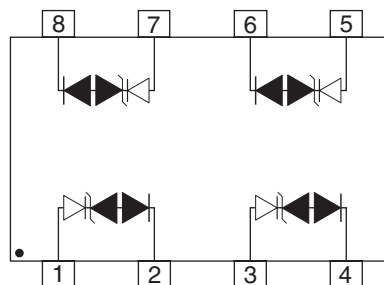
- ✓ 600 Watts Peak Pulse Power per Line ($t_p = 8/20\mu$ s)
- ✓ Provides Protection For Two Line Pairs
- ✓ ESD Protection > 40 kilovolts
- ✓ **LOW LEAKAGE CURRENT < 1.0 μ A**
- ✓ **ULTRA LOW CAPACITANCE: 3pF Typical**

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SO-8
- ✓ Weight 0.6 grams (Approximate)
- ✓ Flammability rating UL 94V-0
- ✓ 12mm Tape and Reel Per EIA Standard 481
- ✓ Device Marking: Marking Code, Logo, Date Code & Pin One Defined By DOT on Package



PIN CONFIGURATION



DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	600	Watts
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{PP}	30	Amps
Lead Soldering Temperature	I_{FRM}	260°C (10s)	°C
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified										
PART NUMBER	DEVICE MARKING CODE	RATED STAND-OFF VOLTAGE (See Note 1)	MINIMUM BREAKDOWN VOLTAGE (See Note 1)	MINIMUM SNAPBACK VOLTAGE (See Note 1)	MAXIMUM CLAMPING VOLTAGE (See Note 1) (See Fig. 2)	MAXIMUM CLAMPING VOLTAGE (See Note 1) (See Fig. 2)	MAXIMUM CLAMPING VOLTAGE (See Note 1) (See Fig. 2)	MAXIMUM CLAMPING VOLTAGE (See Note 1) (See Fig. 2)	MAXIMUM LEAKAGE CURRENT (See Note 1)	TYPICAL CAPACITANCE (See Note 1)
		V_{WM} VOLTS	@ 1mA $V_{(BR)}$ VOLTS	@ $I_{SB} = 50mA$ V_{SB} VOLTS	@ $I_p = 2A$ V_C VOLTS	@ $I_p = 5A$ V_C VOLTS	@ $I_p = 24A$ V_C VOLTS	@ $I_p = 30A$ V_C VOLTS	@ V_{WM} I_D μA	@ 0V, 1MHz C pF
SLVU2.8-4	SL4	2.8	3.0	2.8	5.5	8.5	15	21	1.0	3

Note 1: Device measured between pin 1 to 2, pin 3 to 4, pin 5 to 6 and pin 7 to 8.

GRAPHS

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

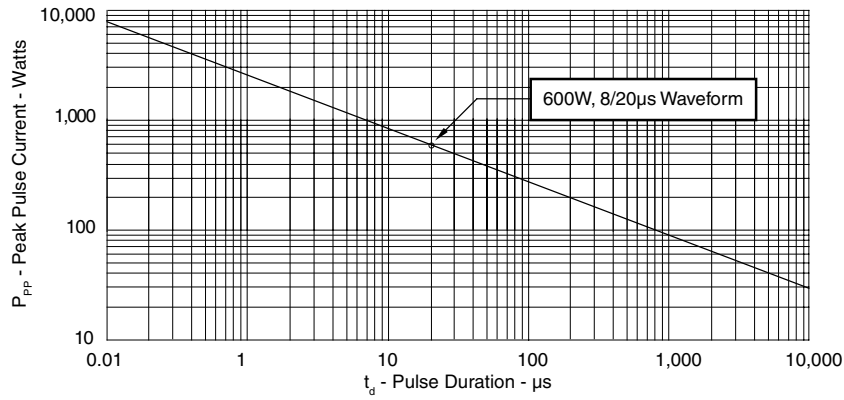


FIGURE 2
PULSE WAVE FORM

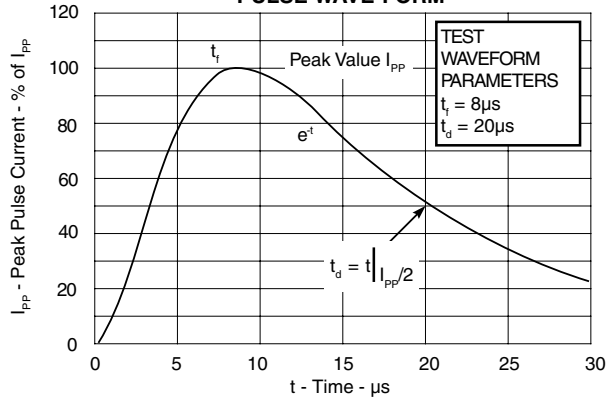


FIGURE 3
POWER DERATING CURVE

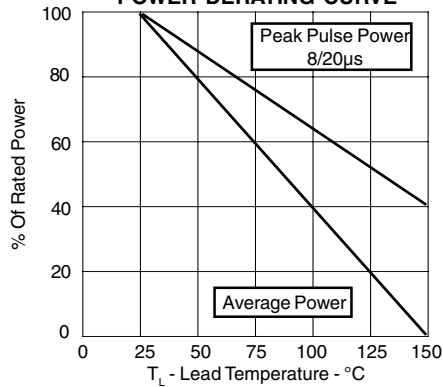
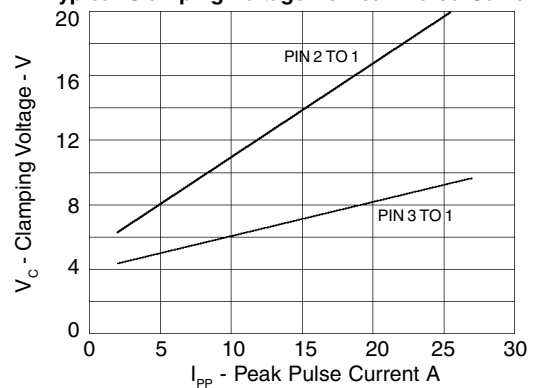


FIGURE 4
Typical Clamping Voltage vs Peak Pulse Current



APPLICATION NOTE

Electronic equipment is susceptible to damage caused by Electrostatic Discharge (ESD), Electrical Fast Transients (EFT), and tertiary lightning effects. Knowing that equipment can be damaged, the SLVU2.8-4 was designed to provide the level of protection required to safe guard sensitive equipment. This product can be used in different configurations to provide a level of protection to meet unidirectional line requirements as well as bidirectional requirements either in a common-mode or differential-mode configuration.

UNIDIRECTIONAL DIFFERENTIAL-MODE CONFIGURATION (Figure 1)

The SLVU2.8-4 provides up to four lines of protection in a differential-mode configuration as depicted in figure 1.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to Pin 1
- ✓ Line 2 is connected to Pin 7
- ✓ Line 3 is connected to Pin 3
- ✓ Line 4 is connected to Pin 5
- ✓ Pins 2, 4, 7 and 8 are connected to ground

BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 2)

The SLVU2.8-4 provides up to two lines of protection in a common-mode configuration as depicted in figure 1.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to Pins 1 & 8
- ✓ Line 2 is connected to Pins 4 & 5
- ✓ Pins 2, 3, 6, and 7 are connected to ground

BIDIRECTIONAL DIFFERENTIAL-MODE CONFIGURATION (Figure 3)

The SLVU2.8-4 provides up to two-line pairs of protection in a differential-mode configuration as depicted in figure 1.

Circuit connectivity is as follows:

- ✓ Line Pair 1 is connected to Pins 1 & 2
- ✓ Line Pair 1 is connected to Pins 7 & 8
- ✓ Line Pair 2 is connected to Pins 3 & 4
- ✓ Line Pair 2 is connected to Pins 5 & 6

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Figure 1. Unidirectional Differential-Mode Protection

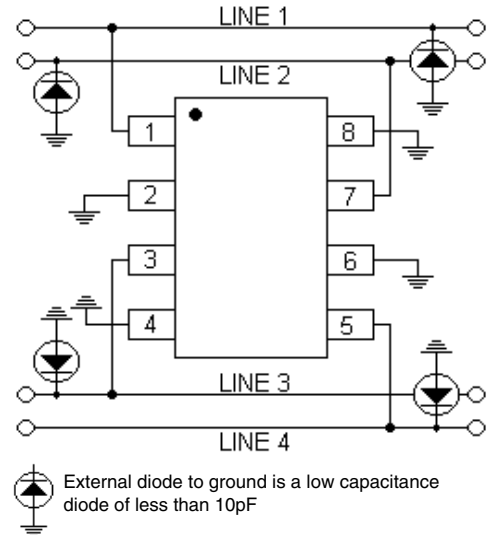


Figure 2. Bidirectional Common-Mode Protection

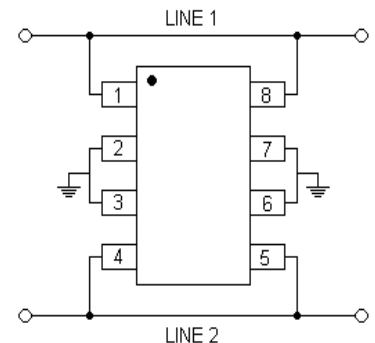
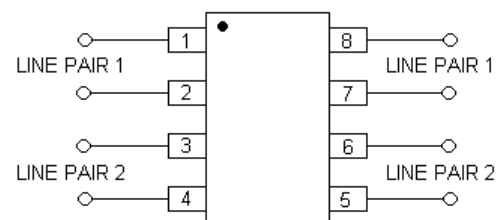
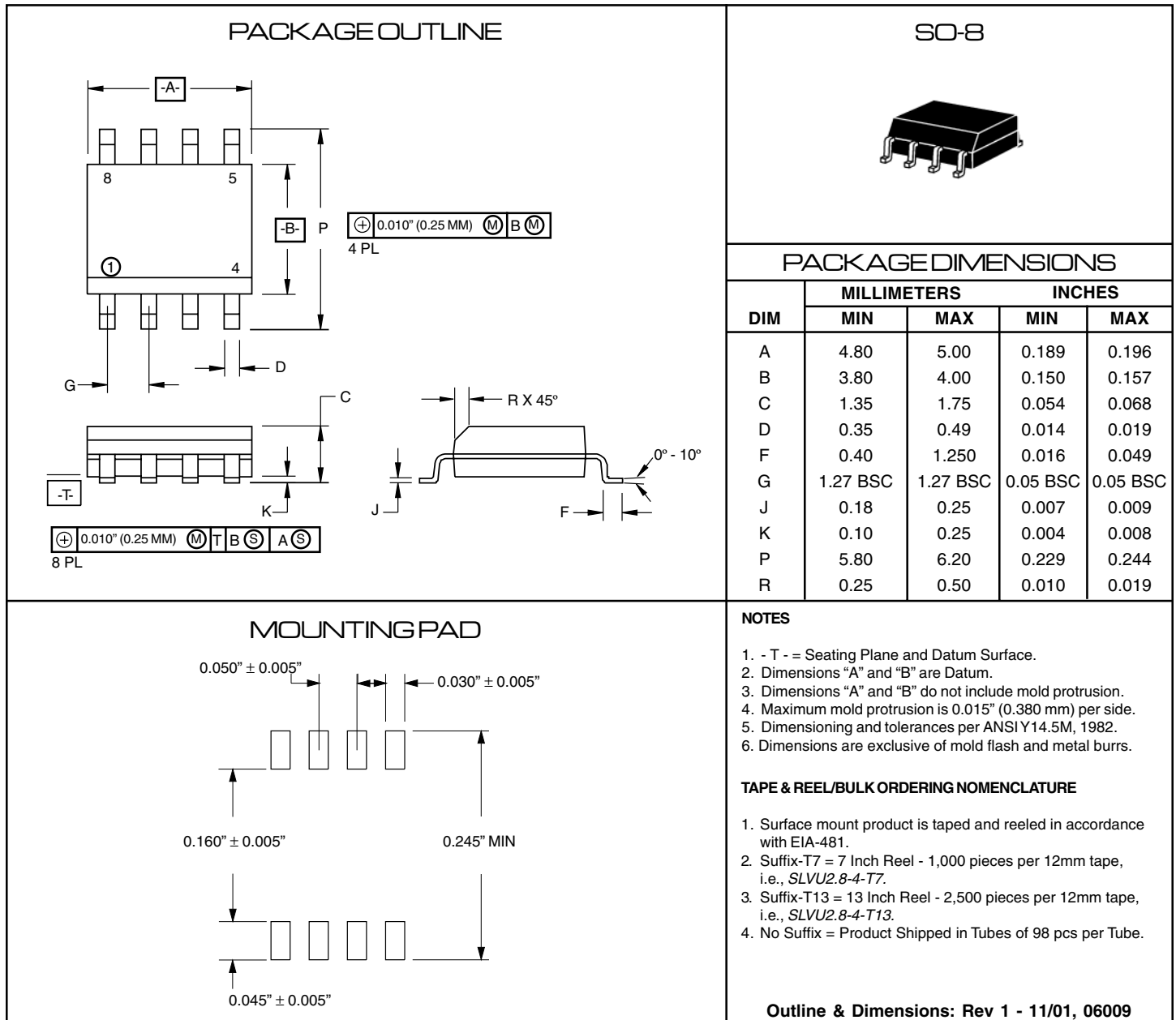


Figure 3. Bidirectional Differential-Mode Protection



PACKAGE OUTLINE & DIMENSIONS



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